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Developing and Understanding Materials Processing-Property Relationships for Carbon Nanotube Electronics

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ABSTRACT

Developing and Understanding Materials Processing-Property Relationships for Carbon Nanotube Electronics

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The commercial success of personal computing has led to the rapid creation and proliferation of diverse electronic systems including desktops, laptops, tablets, mobile devices, and embedded systems. For the past five decades, silicon has served as the base material for computing electronics. However, with increasing demand for unconventional electronics (e.g., ultrathin flexible wearables), new computing platforms are required that meet increasingly diverse mechanical, electronic, and functional requirements. Conventional silicon integrated circuit technology faces significant challenges in meeting these demands due to its limited mechanical flexibility, high temperature processing, and scaling limitations. Emerging alternative computing platforms based on other crystalline semiconductors suffer from similar limitations. Consequently, next-generation electronics necessitates the exploration of radically different electronic materials.

Single-walled carbon nanotubes (SWCNTs) are among the most promising and highly studied nanoelectronic materials. Due to their small size, solution-processability, chemical stability, and chirality-dependent optoelectronic properties, SWCNTs offer a number of unique advantages and are compatible with the complex requirements of future electronic devices. Recent advances in post-processing methods have allowed SWCNTs to be used as semiconducting channels in diverse settings including charge transport devices, optical emitters and detectors, and chemical sensors. With this tunable functionality, a wide range of SWCNT-based electronic applications have been realized, such as printed digitial logic and complementary metal-oxide-

semiconductor (CMOS) field-effect transistors (FETs). Despite this progress, most applications realized to date have largely focused on digital logic, and demonstrations of other key logic and analog functions remain largely unexplored. Moreover, silicon electronics are often used to perform these functions, further limiting the impact of SWCNT-based devices in practical electronic systems. Therefore, SWCNT-based electronics capable of performing these key functions must be realized to fully exploit the potential of solution-processed SWCNTs in emerging electronics. To this end, work presented in this dissertation focuses on the development of materials processing methods and their impact on SWCNT device properties. With this understanding of processing-property relationships, this work demonstrates SWCNT devices with novel function and performance in two key applications, overcoming fundamental challenges in the development SWCNT-based security and sensing technologies.

Innovative materials processing and device operation are at the core of this thesis and have led to the development of the first true random number generator based on a solution-processed semiconductor. Processing optimization of charge transport through tunable doping, encapsulation and transistor design enabled the realization of low-power, complementary SWCNT static random access memory (SRAM) cells. Further characterization of device operation under dynamic biasing conditions allowed for the development of biasing strategies to operate these SWCNT SRAM cells as random bit generators through digitization of thermal noise. This work shows that this approach requires minimal computational overhead to produce highly random bit streams, as is confirmed through a series of rigorous tests including the National Institute of Standards and Technology (NIST) randomness statistical test suite (STS) and the TestU01 battery tests. This thesis work thus overcomes a key application-specific challenge to low cost, flexible security electronics by demonstrating a ubiquitous security primitive using a solution-processed semiconductor. In turn,

this provides a path for improving security in the rapidly growing global network of interconnected electronic and sensing devices.

Further innovative transistor design and understanding of material processing-property relationships led to the development of a novel ohmic-contact-gated transistor (OCGT) using solution-processed SWCNTs. Through the development of a novel self-aligned photolithography technique and processing optimization of components critical in charge transport (i.e., contacts and channel), a key advantage of the OCGT device geometry is realized through gating of the semiconducting channel with both the bottom gate and top contact electrode without the need of additional terminals beyond the conventional gate-source-drain configuration. In turn, this novel transistor design enables unprecedented levels of output current saturation in short channel limits (i.e., channel lengths < 300 nm) using atomically thin semiconductors without compromising the output current drive. Solution-processed SWCNT random networks are used to implement OCGTs that mitigate short channel effects to achieve low output conductance with high output current levels, overcoming the tradeoff relationship that is typically observed in conventional field-effect transistors FETs. These SWCNT OCGTs are then used in common-source amplifiers to attain the highest output current density and length-scaled signal gain to date for amplifiers based on solution-processed semiconductors, overcoming a key challenge in the development of practical sensing technologies. The utility and robustness of these amplifiers is further demonstrated by amplifying a number of analog biological signals from sensors commonly found in Internet of Things (IoT) and medical devices. Because the facile OCGT fabrication design can be generalized to other semiconducting nanomaterials, this thesis work has wide-ranging implications for solution-processed analog electronics.

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LIST OF ABBREVIATIONS

0D	Zero-dimensional
1D	One-dimensional
2D	Two-dimensional
3D	Three-dimensional
ADC	Analog-to-digital converter
AFM	Atomic force microscopy
AI	Artificial intelligence
Al_2O_3	Aluminum oxide, alumina
ALD	Atomic layer deposition
AMOLED	Active-matrix organic light-emitting diode display
ATPE	Aqueous two-phase extraction
BFBD	Barrier-free bipolar-diode
BJT	Bipolar junction transistor
BL	Bitline
BV	Benzyl viologen
CD	Circular dichroism
CMOS	Complementary metal-oxide-semiconductor
CNT	Carbon nanotube
CTOLED	Color-tunable organic light-emitting diode
CVD	Chemical vapor deposition
DC	Direct current

DGU	Density gradient ultracentrifugation
DOPA	3,4-dihydroxyphenylalanine
DPV	Differential pulse voltammetry
DX	Dextran
EBL	Electron beam lithography
ECG	Electrocardiogram
EL	Electroluminescence
EMG	Electromyography
EPSC	Excitatory post-synaptic current
FESA	Floating evaporative self-assembly
FET	Field-effect transistors
FFT	Fast Fourier transform
FMN	Flavin mononucleotide
FWHM	Full width at half maximum
GC	Gel chromatography
GCE	Glassy carbon electrode
GND	Ground
g_m	Transconductance
g_o	Output conductance
hBN	Hexagonal boron nitride
HfO_2	Hafnium (IV) oxide, hafnia
IC	Integrated Circuit
I_{DS}	Drain current

$I_{DS,max}$	Maximum drain current
I_{DS}-V_{DS}	Output
I_{DS}-V_{GS}	Transfer
I_{off}	Off current
I_{on}	On current
IoT	Internet of Things
IR	Infrared
JNFET	Junction-less nanowire field-effect transistor
L	Field-effect transistor channel length
MoS_2	Molybdenum disulfide
m-SWCNT	Metallic single-walled carbon nanotube
NIST	National Institute of Standards and Technology
NMOS	n-channel metal-oxide-semiconductor
NMP	N-methyl-2-pyrrolidone
NMPI	4-(N-hydroxycarboxamido)-1-methylpyridinium iodide
O_2	Oxygen
OCGT	Ohmic-contact-gated transistor
OLED	Organic light-emitting diode
PAM	Polyacrylamide
PCz	Poly[9-(1-octylonoyl)-9H-carbazole-2,7-diyl]
PDLC	Polymer-dispersed liquid crystals
PDMS	Polydimethylsiloxane
PECVD	Plasma-enhanced chemical vapor deposition

PEG	Poly(ethylene glycol)
PEN	Polyethylene naphthalate
PET	Poly(ethylene terephthalate)
PFO-BPy	Poly[(9,9-dioctylfluorenyl-2,7-diyl)-*alt*-*co*-(6,6'-[2,2'-bipyridine])]
PL	Photoluminescence
PMMA	Poly(methyl methacrylate)
PMOS	p-channel metal-oxide-semiconductor
pMSSQ	Poly(methyl silsesquioxane)
PPG	Photoplethysmogram
PSR	Pressure-sensitive rubber
PUF	Physically unclonable function
PVA	Polyvinyl alcohol
PVP	Poly(vinylphenol)
R2R	Roll-to-roll
RH	Relative humidity
RIE	Reactive ion etching
RO	Ring oscillator
r_o	Output resistance
RRAM	Resistive random-access memory
SCALE	Self-aligned capillary-assisted lithography for electronics
SEBS	Styrene-ethylene-butadiene-styrene
SEM	Scanning electron microscope

SGT	Source-gated transistor
SMU	Source-measurement unit
SNN	Spiking neural network
SPE	Single photon emission
SRAM	Static random-access memory
SS	Subthreshold swing
ss-DNA	Single-stranded DNA
STDP	Spiking-time dependent plasticity
STS	Statistical test suite
SWCNT	Single-walled carbon nanotube
s-SWCNT	Semiconducting single-walled carbon nanotube
TDMAH	Tetrakis(dimethylamido)hafnium(IV)
TMAl	Trimethylaluminum
TEM	Transmission electron miscroscope
TID	Total ionization dose
TFT	Thin-film transistor
TRNG	True random number generator
UV	Ultraviolet
VCO	Voltage-controlled oscillator
V_{DS}	Drain-source voltage
V_{DD}	Supply voltage
VEGT	Vertical electrolyte-gated transistor
V_{GS}	Gate-source voltage

V_{IN}	Input voltage
VLSI	Very-large-scale-integration
V_{OUT}	Output voltage
V_{TH}	Threshold voltage
W	Field-effect transistor channel width
WL	Wordline
μ_{FE}	Field-effect mobility

Dedicated to my family and my girls

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

Chapter 1: Introduction to carbon nanotubes

For the past half century, silicon has served as the primary material platform for integrated circuit technology. However, the recent proliferation of non-traditional electronics, such as wearables, embedded systems, and low-power portable devices, has led to increasingly complex mechanical and electrical performance requirements. Among emerging electronic materials, single-walled carbon nanotubes (SWCNTs) are promising candidates for next-generation computing as a result of their superlative electrical, optical, and mechanical properties. Moreover, their chirality-dependent properties enable a wide range of emerging electronic applications including sub-10 nm complementary field-effect transistors, optoelectronic integrated circuits, and enantiomer-recognition sensors. In this section, we review recent progress in SWCNT-based computing devices, with an emphasis on the relationship between chirality enrichment and electronic functionality. In particular, we highlighting chirality-dependent SWCNT properties and chirality enrichment methods, summarizing the range of computing applications that have been demonstrated using SWCNTs to date.

1.1 SWCNTs in modern electronics

The commercial success of personal computing has led to the rapid creation and proliferation of diverse electronic systems including desktops, laptops, tablets, mobile devices, and embedded systems. For the past five decades, silicon has served as the base material for computing electronics.[1] However, with increasing demand for unconventional electronics (e.g., ultrathin flexible wearables), new computing platforms are required that meet increasingly diverse mechanical,[2] electronic,[3,4] and functional requirements.[5] Conventional silicon integrated circuit technology faces significant challenges in meeting these demands due to its limited mechanical flexibility, high temperature processing, and scaling limitations. Emerging alternative computing

platforms based on other crystalline semiconductors suffer from similar limitations. Consequently, next-generation computing necessitates the exploration of radically different electronic materials.

Single-walled carbon nanotubes (SWCNTs) are among the most promising and highly studied nanoelectronic materials. Due to their small size,[6,7] solution-processability,[8] chemical stability,[9] and chirality-dependent optoelectronic properties,[10] SWCNTs offer a number of unique advantages and are compatible with the complex requirements of future computing devices. Recent advances in chiral enrichment of polydisperse SWCNTs[8,10] have allowed their use as semiconducting channels in diverse settings including charge transport devices,[2] optical emitters and detectors,[11,12] and chemical sensors.[2,3,13,14] With this tunable functionality, a range of SWCNT-based computing applications have been realized, such as printed digital logic,[15] sub-10 nm complementary metal-oxide-semiconductor (CMOS) field-effect transistors (FETs),[16] neuromorphic devices,[17] single-photon emitters,[18] and enantiomer-recognition sensors.[14]

In this section, we discuss recent advances in SWCNT-based computing technologies that process, manage, and communicate information, with an emphasis on the enabling role of chiral enrichment. Section 1.2 defines the different levels of chiral enrichment. Sections 1.3 and 1.4 describe direct growth methods and post-processing purification of SWCNTs for electronic-type and monochiral enrichment. Section 2.1 discusses applications of electronic-type-enriched SWCNTs such as wearables, highly-scaled FETs, three-dimensional (3D) logic-memory integration, and neuromorphic devices. Section 2.2 outlines applications of monochiral-enriched SWCNTs including monochiral FETs, optical emitters, photodetectors, and optoelectronic integrated circuits (ICs). Finally, Section 2.3 considers recent progress towards enantiomerically-pure SWCNTs.

1.2 SWCNT electronic properties

SWCNTs and graphene are carbon allotropes consisting of sp^2-bonded carbon atoms. While graphene consists of a planar layer of carbon atoms in a honeycomb lattice arrangement, a SWCNT can be thought of as a single sheet of graphene rolled to form a seamless, hollow cylinder. Most properties of a SWCNT are determined by the rolling direction with respect to the graphene lattice, which is referred to as the SWCNT chiral vector. As shown in Figure 1.1, the chiral vector is defined with respect to the basis vectors ($\mathbf{a_1}$, $\mathbf{a_2}$) such that each SWCNT structure is identified by a pair of chiral indices (*n,m*). The SWCNT structures shown in Figure 1.1 are generated using the TubeGen 3.4 web interface.[19] Typically, SWCNTs have a diameter of less than 2 nm, with lengths in the range of 1-2 μm. Given their high aspect ratios, SWCNTs are commonly classified as one-dimensional nanostructures.

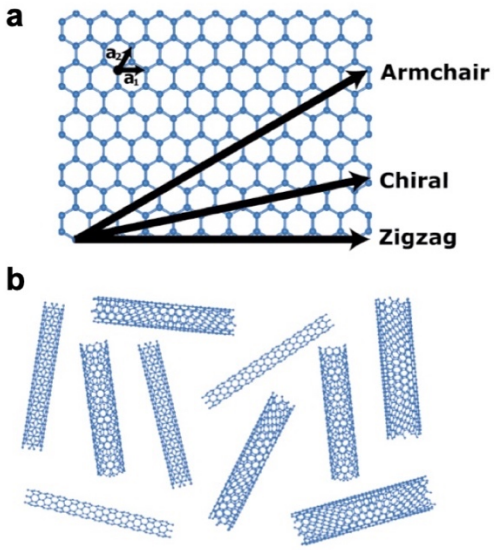

Figure 1.1 | Unsorted SWCNTs. a, Diagram of a graphene sheet with basis vectors (a1, a2) and common chiral vectors used to define SWCNTs. **b,** Conceptual illustration of as-produced raw, unsorted SWCNTs with numerous chiralities. These SWCNT structures were generated using the TubeGen 3.4 web interface.[19] Reproduced with permission.[20] Copyright 2020, Wiley-VCH Verlag GmbH & Co. KGaA, Weinheim.

Despite their desirable mechanical, chemical, and thermal properties, SWCNTs are primarily utilized for their excellent charge transport properties. These electronic properties vary as a function of the chiral vector. Specifically, an (*n,m*) SWCNT will be semiconducting if $n - m \neq 3z$ (where z is an integer) and metallic otherwise. Therefore, for samples consisting of a random distribution of chiral vectors, approximately 33% of the SWCNTs will be metallic and 67% will be semiconducting, with the semiconducting bandgap inversely proportional to the SWCNT diameter.[9] Semiconducting SWCNTs (s-SWCNTs) are preferred in most electronic applications, but often require semiconducting purity levels higher than 99% (Figure 1.2).[1] On the other hand, optoelectronic applications generally require enrichment of a single (*n,m*) chirality due to the diameter dependence of the SWCNT bandgap (Figure 1.3). As an additional degree of freedom, individual (*n,m*) SWCNTs are also defined by their handedness (M: left-handed, P: right-handed), which can be thought of as the two possible rolling directions for (*n,m*) SWCNT enantiomers. SWCNT handedness influences interactions with other chiral species (e.g., biomolecules) and circularly polarized light,[21] making it a crucial property for a number of advanced sensing applications (Figure 1.4).

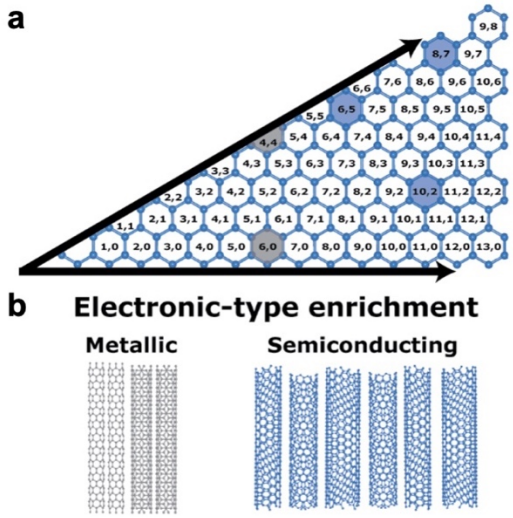

Figure 1.2 | SWCNTs sorted by electronic type. Illustration of electronic-type enrichment of raw SWCNTs. SWCNTs are separated into metallic and semiconducting species (**b**), with their corresponding chiral vectors highlighted in the chiral map (**a**). These SWCNT structures were generated using the TubeGen 3.4 web interface.[19] Reproduced with permission.[20] Copyright 2020, Wiley-VCH Verlag GmbH & Co. KGaA, Weinheim.

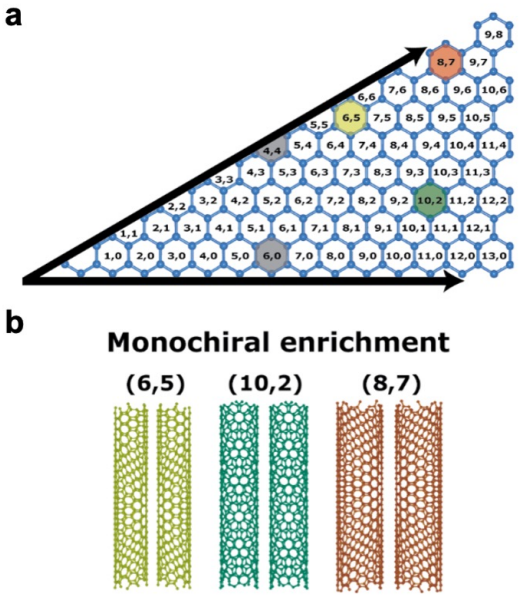

Figure 1.3 | SWCNTs sorted by chirality. Illustration of monochiral enrichment of semiconducting SWCNTs. Semiconducting SWCNTs are separated by chirality (**b**), with their corresponding chiral vectors highlighted (**a**). These SWCNT structures were generated using the TubeGen 3.4 web interface.[19] Reproduced with permission.[20] Copyright 2020, Wiley-VCH Verlag GmbH & Co. KGaA, Weinheim.

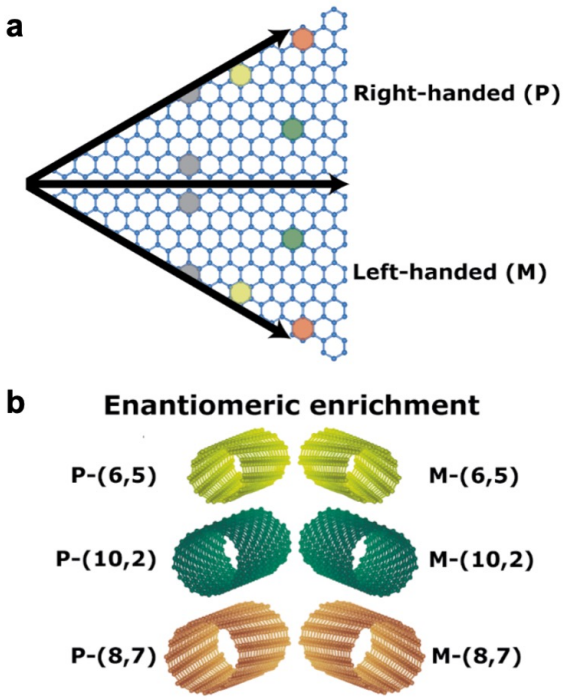

Figure 1.4 | SWCNTs sorted by chirality and handedness. Illustration of enantiomeric enrichment of monochiral SWCNTs. Monochiral SWCNTs are separated into right-handed (P) and left-handed (M) species (**b**) with their corresponding chiral vectors highlighted (**a**). These SWCNT structures were generated using the TubeGen 3.4 web interface.[19] Reproduced with permission.[20] Copyright 2020, Wiley-VCH Verlag GmbH & Co. KGaA, Weinheim.

1.3 SWCNT direct growth

Since the first demonstration of SWCNT synthesis in 1993,[6] researchers have explored the direct growth of SWCNTs with controlled structure (most commonly chirality, but also length and alignment). SWCNT growth depends on a broad number of synthetic parameters including substrate, temperature, pressure, and carbon source. However, it is generally believed that catalyst chemistry has the largest effect since chirality is dictated by initial nucleation during growth.[10] Most chirality-enriched direct growth methods can be classified into the following three categories: (1) carbonaceous molecular precursors; (2) metallic nanoparticles; (3) SWCNT fragments as growth seeds. We briefly discuss these three categories, and refer the reader to the

following comprehensive review articles for direct growth chirality control,[10,22,23] horizontal alignment,[24,25] catalyst design,[26] and epitaxy.[27]

In direct growth using carbonaceous molecular precursors, synthetic organic chemistry is used to develop templates for SWCNT growth. Carbonaceous templates, such as end-cap precursors and carbon nanorings, are designed to have a molecular structure at their nucleation site that is identical to the target SWCNT chirality. In a notable demonstration of this strategy, corannulene molecules are used in the bottom-up synthesis of (5,5) SWCNT end-caps.[28] These molecules are then deposited on quartz substrates, and SWCNT growth is achieved using vapor phase epitaxy elongation. A schematic of the end-cap structure as well as a scanning electron microscope (SEM) image of the SWCNT growth are provided in Figure 1.5. Despite the atomically precise precursor design, characterization of the grown SWCNTs reveals a change in chirality during growth. This setback is representative of the challenges facing direct growth through carbonaceous molecular precursors, and highlights the need for further growth optimization. Even with these challenges, this methodology offers a number of promising advantages including metal-free catalyst growth and the potential for scalability through the use of high-throughput organic synthesis of identical templates.[10,26,29]

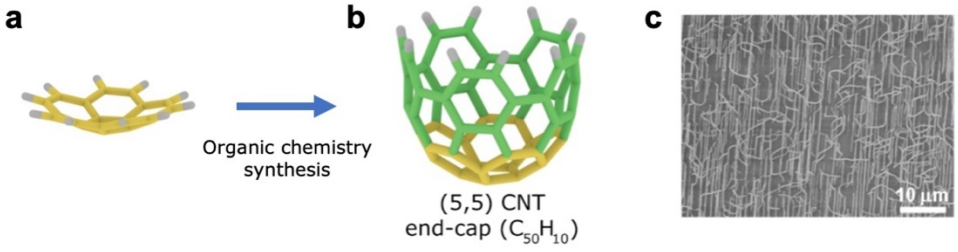

Figure 1.5 | SWCNT growth using molecular templates. a, Structure of synthetic $C_{20}H_{10}$ precursor for SWCNT growth. **b,** Structure of a $C_{50}H_{10}$ molecular end-cap with a short segment of monochiral SWCNT following organic chemistry synthesis of precursor. **c,** SEM image of

SWCNTs grown using molecular end-cap templates on a quartz substrate. Reproduced with permission.[28] Copyright 2018, Wiley-VCH Verlag GmbH & Co. KGaA, Weinheim.

In direct growth using metallic nanoparticles, transition metals (e.g., Co, Fe, and Ni) are used due to their high catalytic activities for the dissociation of carbon precursors.[23,30] Metallic nanoparticle catalysts with carefully designed size and composition are formed on the growth substrate, after which SWCNT synthesis is achieved through carbon adsorption, nucleation, and elongation via chemical vapor deposition (CVD).[26] In one example of this method, CVD is performed on an ST-cut single quartz crystal with Fe catalyst strips. During synthesis, an alternating electric field is applied as shown in Figure 1.6, resulting in nucleation that produces horizontally aligned SWCNTs with 99.9% semiconducting purity.[31] Generally, the thermodynamics and kinetics of this growth method are highly sensitive to the catalyst properties, such that ideal conditions for chiral-selective growth require simultaneous control over a large number of growth parameters.[22,24,25] Consequently, advances to date have required extensive theoretical studies and/or significant experimental optimization.[10,25]

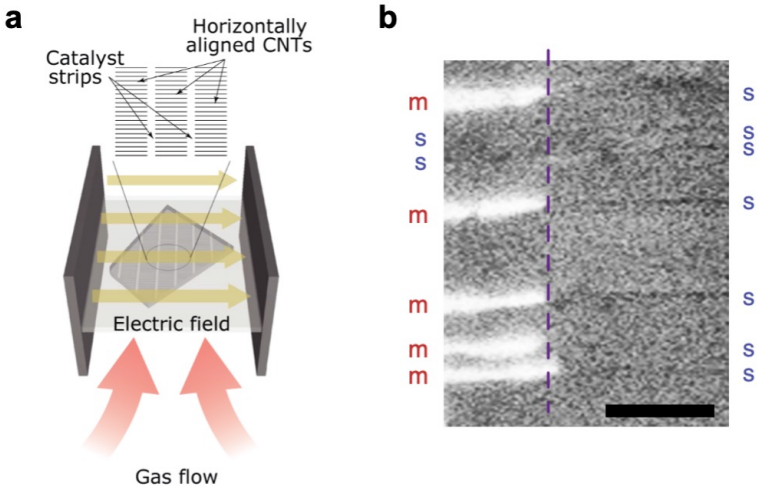

Figure 1.6 | SWCNT growth using electro-renucleation. a, Diagram of an electro-renucleation system that utilizes metallic catalyst strips on a quartz crystal placed between two electrodes for controllable CVD growth using an alternating electric field. **b,** SEM image of SWCNTs

changing chirality during growth when electro-renucleation starts (dashed purple line). Bright and dark lines represent m-SWCNTs and s-SWCNTs, respectively. Reprinted by permission from Springer Nature: Nature Catalysis,[31] Copyright (2018).

In direct growth using SWCNT fragments, open-ended SWCNTs serve as seeds that are elongated through epitaxial growth. Studies using this technique have confirmed that elongated SWCNTs maintain the original seed chirality. In one example of this growth method, SWCNT seeds are placed on a Si/SiO_2 substrate, and their growth edges are activated through exposure to microwave irradiation. Subsequent CVD growth from these activated SWCNTs results in synthesis with high regeneration efficiency and micron-scale elongation. An overview of this method is shown in Figure 1.7.[32] Further optimization of the microwave-assisted activation may help overcome the typical low yield and growth efficiency of SWCNT-seeded growth that is currently limited by spontaneous closure of the growth seed edge.[27] When coupled with recent advances in post-processing purification that will be delineated in the next section, this growth method has the potential to provide large-scale chirality enrichment.[10,27]

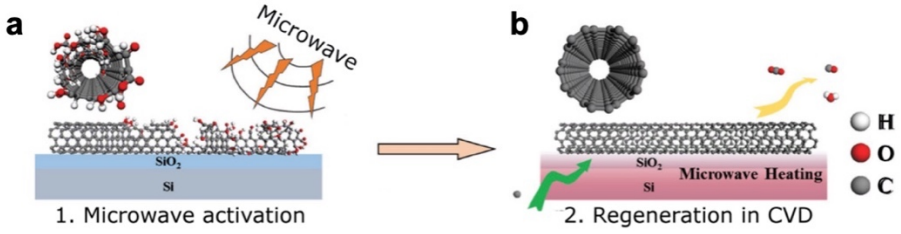

Figure 1.7 | SWCNT growth using microwave-assisted regeneration. Schematic of microwave-assisted regeneration growth using irradiated SWCNT fragments (**a**) as growth seeds for regenerative growth using CVD (**b**). Reproduced with permission.[32] Copyright 2018, Wiley-VCH Verlag GmbH & Co. KGaA, Weinheim.

1.4 SWCNT post-processing purification

Despite the aforementioned advances in direct growth, post-processing purification is currently the more common route to SWCNT chiral enrichment. Due to the similarity in size between SWCNTs and biological macromolecules, many post-processing purification techniques draw inspiration from biotechnology separation methods.[8] Among the most successful post-processing techniques are: (1) dielectrophoresis; (2) polymer sorting; (3) aqueous two-phase extraction; (4) density gradient ultracentrifugation; (5) gel chromatography. We briefly discuss these five post-processing purification methods, and refer the reader to the following comprehensive reviews for electronic-type[8] and monochiral[33,34] enrichment. We also highlight that the following references[33,34] compare the scalability, applicability, enrichment levels, and performance of the post-processing purification methods discussed below. Post-processing purification for enantiomeric enrichment will be discussed in Section 2.3.

In dielectrophoresis, an alternating voltage is applied using planar electrodes to create a local, inhomogeneous electric field. Due to a difference in induced dipole moment between semiconducting and metallic species, s-SWCNTs suspended in solution near the electrodes selectively interact with the inhomogeneous electric field, resulting in preferential deposition. While early demonstrations of this method suffered from poor selectivity and non-uniform deposition,[35] near perfect alignment and uniform pitch have been more recently achieved through optimization of the fringing electric field.[36] A diagram of the dielectrophoresis process and an SEM image of the resulting uniform SWCNT arrays are provided in Figure 1.8. Electrophoretic methods can be scaled through the use of a dielectric medium (e.g., agarose gel electrophoresis) achieving yields up to 25%.[37] However, these scalable methods have only attained electronic-type purities up to 98%, have not demonstrated monochiral selectivity, and require additional post-

processing for the removal of agarose gels,[34,38] thus limiting the adoption of electrophoretic methods compared to other post-processing purification methods.

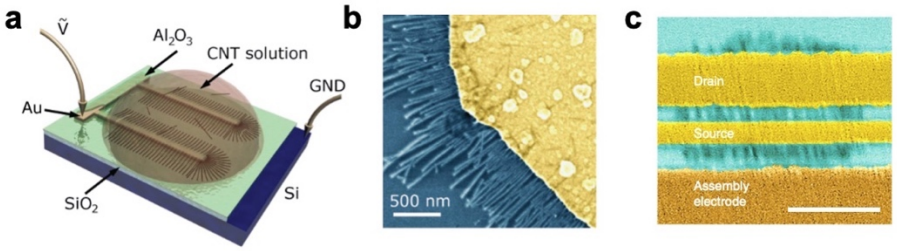

Figure 1.8 | SWCNT sorting using dielectrophoretic assembly. a, Diagram of fringing-field assembly process using an alternating voltage input for self-limited pitch placement of semiconducting SWCNTs using fringing-field dielectrophoretic assembly. **b,** False-colored SEM image of assembled SWCNT arrays on an electrode. **c,** False-colored SEM image of FET using dielectrophoretic assembly to place s-SWCNTs as a channel between a drain and source electrode (500 nm scale bar). Reprinted by permission from Springer Nature: Nature Communications,[36] Copyright (2014).

In polymer sorting, tailored polymers selectively interact with SWCNTs based on properties such as diameter, length, electronic type, and chirality. Although the precise sorting mechanism remains debatable, this selective interaction creates a dispersion that can be separated from a bulk mixture using solution processing, most often through centrifugation.[39] In a notable example of polymer sorting, high-speed shear force mixing is used to disperse poly[(9,9-dioctylfluorenyl-2,7-diyl)-*alt-co*-(6,6'-[2,2'-bipyridine])] (PFO-BPy) and SWCNTs in a toluene solution. This polymer produces large volumes of nearly monochiral SWCNT dispersions, with s-SWCNT purity above the optical characterization detection limit (>99%) and (6,5) SWCNT content above 84%.[40] Figure 1.9 shows the structure of PFO-BPy and (6,5) SWCNTs, as well as the optical absorption spectra of dispersions after sequential recycling of unwrapped material. A number of other distinct sorting polymers with unique functionality have been developed, including polymers that can achieve ultrahigh purity electronic-type enrichment,[8,41] and polymers

that can be recycled to minimize production costs.[42,43] Polymer sorting remains an effective method for state-of-the-art electronic-type enrichment, achieving semiconducting purities above 99.9% and yields above 20%.[15,34,41,42] Although monochiral enrichment purities are significantly lower (50-84%), polymer sorting is compatible with large-scale and iterative solution-processing methods,[33,40,44] suggesting that it may be able to achieve higher levels of monochiral enrichment.

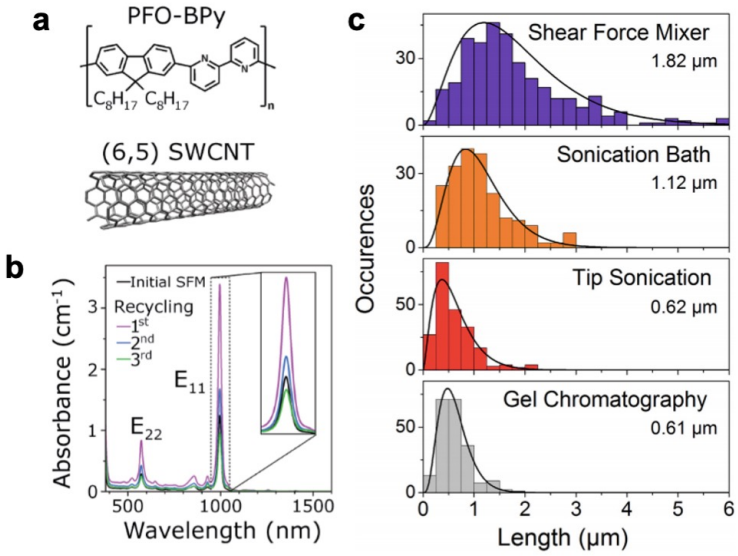

Figure 1.9 | SWCNT sorting using polymer-wrapping. a, Structure of the sorting copolymer PFO-BPy and the target monochiral (6,5) SWCNT. **b,** Evolution of the absorption spectra of (6,5) SWCNT-copolymer dispersions after sequential recycling of unwrapped material from selective dispersion of (6,5) SWCNTs using high-speed shear force mixing. **c,** Length distribution of (6,5) SWCNTs using shear force mixing, bath sonication, tip sonication and gel chromatography. Reprinted from [40], Copyright (2016), with permission from Elsevier under CC BY NC ND.

In aqueous two-phase extraction (ATPE), two water-soluble polymers are mixed, spontaneously creating two distinct immiscible phases. Using the poly(ethylene glycol) (PEG) / dextran (DX) system, the immiscible phases allow for the selective extraction of SWCNT species due to their different affinities for SWCNTs based on diameter, length, electronic-type, chirality,

and surface chemistry (e.g., surfactants). In a notable demonstration, ATPE using the PEG/DX system achieved monochiral separation of SWCNTs in three processing steps, thus enabling the separation of 11 small-diameter SWCNT chiralities using amphiphilic surfactants.[45] A schematic of the processing steps and the resulting optical absorption spectra of the separated SWCNT chiralities are provided in Figure 1.10. ATPE has also been used for the separation of up to 15 different SWCNT chiralities using specific DNA sequences for partitioning[46] with exceptionally high fidelity.[47] ATPE can achieve state-of-the-art semiconducting purities above 99.5%[48] and monochiral enrichment purities above 85%.[49] Consequently, ATPE has the potential for high scalability, although efficient removal of impurities from the isolated SWCNT species remains an open challenge.[8,34]

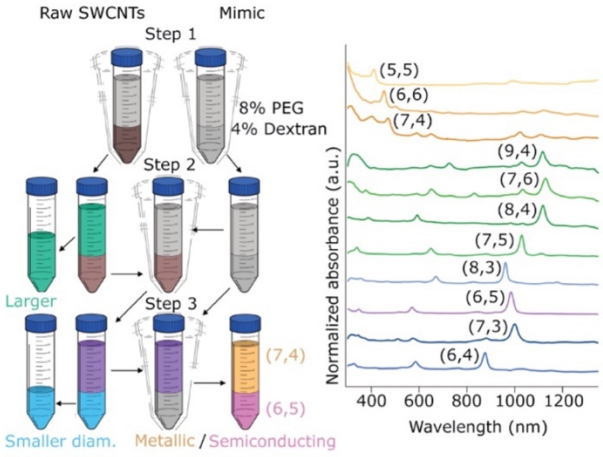

Figure 1.10 | SWCNT sorting using ATPE. Separation of SWCNT chiral species using three-step ATPE. (left) Schematic of the ATPE procedure for the separation of two monochiral species. (right) Absorption spectra of 11 extracted SWCNT monochiral species. Reprinted with permission from [45]. Copyright 2019 American Chemical Society.

In density gradient ultracentrifugation (DGU), the buoyant density of SWCNT species is controlled using selective dispersants. SWCNTs are then separated into different layers through the use of a density gradient medium and ultracentrifugation.[9] While initial efforts enabled DGU

separation by SWCNT electronic-type and diameter,[50] subsequent work on orthogonal iterative DGU resulted in nearly monochiral separation.[51] Examples of separation by diameter, electronic type, and chirality through orthogonal iterative DGU are illustrated in Figure 1.11. Due to the high selectivity and iterative nature of DGU, semiconducting purities above 99%[51,52] and monochiral enrichment purities above 88%[53] have been achieved in a manner that is readily scalable for industrial applications.[8,34]

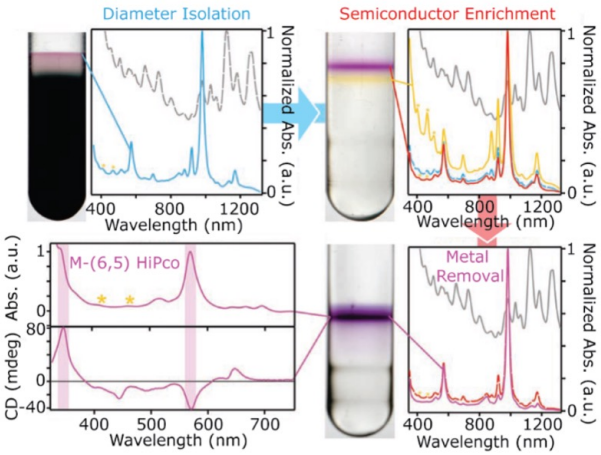

Figure 1.11 | SWCNT sorting using DGU. Optical absorbance spectra, circular dichroism (CD) characterization, and optical photographs showing multiple DGU iterations for electronic-type, monochiral, and enantiomeric enrichment. Reproduced with permission.[51] Copyright 2011, Wiley-VCH Verlag GmbH & Co. KGaA, Weinheim.

In gel chromatography (GC), SWCNT dispersions are separated as they pass through gel columns by exploiting the selective interactions between SWCNTs species and various stationary phases. Through the use of different dispersants and gels, GC can separate SWCNTs by diameter, length, electronic type, and chirality.[8] In one notable example, the use of a single surfactant (i.e., sodium dodecyl sulfate) and multiple gel columns enabled the GC separation of 13 SWCNT chiralities with purities in the range of 46-93%.[54] A schematic of this GC method and photographs of the separated SWCNT species are shown in Figure 1.12. The compatibility of GC with iterative

processing has allowed electronic-type enrichment purity up to 99.9%.[55] GC using ion exchange with single-stranded DNA (ss-DNA) is also capable of sorting SWCNTs by diameter, electronic type, and chirality.[34,56] Since GC has demonstrated large-volume electronic-type and monochiral enrichment with high yields and purity levels,[57] it also has high potential for industrial-scale applications.

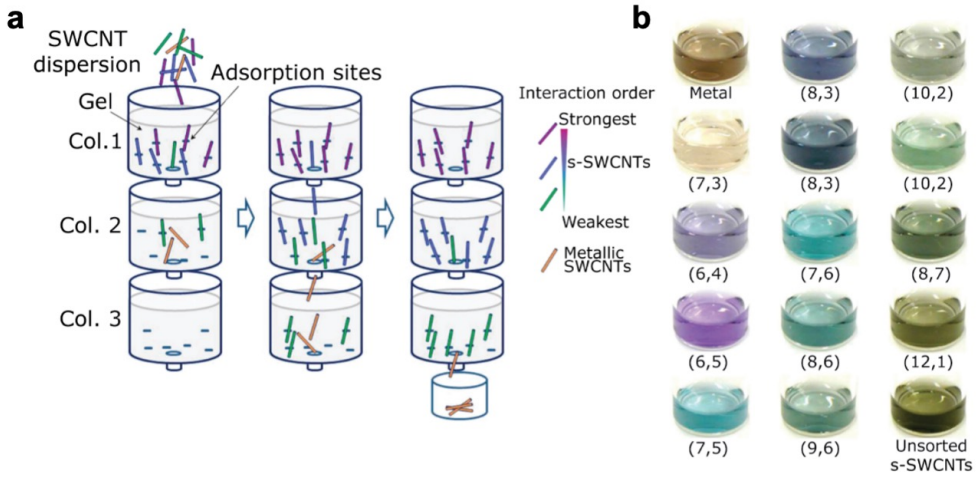

Figure 1.12 | SWCNT sorting using gel chromatography. a, Schematic of single-surfactant multicolumn gel chromatography that enables separation of SWCNT monochiral species. **b,** Photographs of 13 separated monochiral species. Reproduced from[54], licensed by CC BY-NC-SA 3.0.

Chapter 2: Carbon nanotube electronic devices

2.1 Electronic applications of semiconducting SWCNTs

2.1.1 Flexible smart devices

2.1.1.1 Additive manufacturing of flexible SWCNT devices

A key advantage of SWCNTs, in addition to excellent charge transport properties, is their solution processability that enables the use of additive manufacturing techniques, most notably aerosol and inkjet printing. Combined with low-temperature processing and their ultrathin nature, SWCNT-based devices enable flexible computing applications with negligible performance dependence on mechanical deformation.[2] In this section, we briefly discuss a number of key advances in the additive manufacturing of SWCNT devices.

The most common formulations for SWCNT inks employ aqueous surfactant solutions, polymer wrapping, and select organic solvents, which closely follow dispersion strategies in post-processing purification methods.[58] Although not as important for aerosol jet printing, ink viscosities in the ranges of 40 – 2,000 centipoise and 1 – 20 centipoise are required for gravure and inkjet printing, respectively. SWCNT inks are most commonly used to deposit randomly oriented SWCNT networks with feature sizes larger than 5 μm, where uniformity in SWCNT density is critical. Therefore, printing is often aided by surface modification methods,[59,60] where inks are designed to optimize dispersion uniformity and wettability.[3] We refer the reader to the following comprehensive review for further information on SWCNT-based dispersions and printing techniques for flexible SWCNT devices.[3]

In aerosol jet printing, s-SWCNTs inks are aerosolized and printed through a small nozzle using a sheath of inert gas. Although studies generally focus on the charge transport properties of aerosol jet printed s-SWCNT channels, printed contacts also play an important role in overall FET

performance. Fully aerosol jet printed devices have been studied using different contact geometries (e.g., top, bottom, and double) and contact materials including metallic (e.g., Au and Ag) nanoparticles and metallic SWCNTs (m-SWCNTs). It has been found that m-SWCNTs have the lowest contact resistance, especially in the double contact geometry.[59] The performance of an all-printed SWCNT thin-film transistor (TFT) has also been characterized, using s-SWCNT ink for the semiconducting channel, Ag nanoparticle ink for the electrodes, and poly(vinylphenol)/poly(methyl silsesquioxane) (PVP/pMSSQ) for the gate dielectric. With a top-gated structure on a Kapton film, ambient-stable p-type TFTs have been realized with negligible hysteresis and minimal performance variation over 1,000 bending cycles.[61]

In inkjet-printing, s-SWCNTs inks are formulated such that ink droplets can be ejected by a nozzle with precise control over the jetting speed, droplet size, and droplet shape. In one demonstration, SWCNT TFTs were fabricated on flexible polyimide substrates using s-SWCNT ink for the semiconducting channel and Ag nanoparticle ink for the electrodes. The gate dielectric of Al_2O_3 was deposited using atomic layer deposition (ALD), resulting in a change of the TFT transfer characteristics from p-type to ambipolar. This ambipolarity enabled complementary-like ICs including a NAND gate, a NOR gate, and a 3-stage ring oscillator (RO).[62] The RO structure operated continuously for 83 hours with minimal performance variation[62] and allowed the sensing of polar vapors (e.g., acetone),[63] demonstrating the high stability and functionality of this inkjet printing scheme. Although most inkjet-printed SWCNT TFTs have channel lengths larger than 10 μm due to limitations in printing resolution, the fabrication of a fully inkjet-printed TFT with a sub-micron channel length has also been achieved. In this case, a hydrophobic, self-assembled monolayer was applied to an Au nanoparticle electrode to repel a subsequent overlapping printed

electrode. This second electrode thus retracts from the functionalized surface, creating a sub-micron gap of ~400 nm between the two electrodes after printing. Using an ion gel as the gate dielectric, these highly-scaled TFTs achieve simultaneously large ON currents of ~4.5 $\mu A \cdot \mu m^{-1}$, high ON/OFF ratios of ~10^5, and low-voltage operation (V_{DS} = -0.1 V and V_G = -1.5 V).[64] While high-throughput, high-resolution printing remains challenging, the self-aligned capillary-assisted lithography for electronics (SCALE) method provides a path to overcome this bottleneck. SCALE combines inkjet printing with imprint lithography by depositing inks into patterned imprints on a flexible substrate, such that the inks flow from ink reservoirs to narrow cavities through capillary forces. High-resolution SWCNT TFTs have been achieved by using inks for the channel, electrodes, and gate dielectric, including s-SWCNT ink for the semiconducting channel.[65]

Other studies have demonstrated shape-controlled substrates,[66] intrinsically stretchable transistors,[67] and high-throughput fabrication using a photosensitive dry film.[68] In shape-controlled substrates, SWCNT flexible electronic devices are fabricated on a bilayer of polyimide and a shape memory polystyrene structure. These structures are formed into free-standing three-dimensional shapes through structural pre-programming, and can also conformably wrap around irregularly shaped objects through rapid heating. Embedded SWCNT TFTs, sensors, and memory devices in these structures show no significant performance degradation when mechanically deformed.[66] Intrinsically stretchable, all-carbon transistors have also been achieved using transfer printing of a s-SWCNT channel, m-SWCNT electrodes, and a non-polar elastomer dielectric and substrate. A non-polar dielectric is used to minimize hysteresis and stress bias effects in the transistors, while optimized SWCNT source electrodes help achieve transistor performance comparable to conventional SWCNT transistors on rigid substrates.[67] In a high-throughput fabrication approach,

a photosensitive dry film (DuPont Riston MX9010) is laminated on a flexible polyethylene naphthalate (PEN) substrate using roll-to-roll (R2R) technology. The resulting film is then used as a negative photolithography resist layer, which enables a 5 μm pattern resolution over the area of an A5-paper-sized PEN substrate through conventional UV exposure. Flexible and transparent all-carbon TFTs are then fabricated using a poly(methyl methacrylate) (PMMA) dielectric layer and SWCNTs for the channel and electrodes. TFTs and inverters fabricated with this scheme have attained high performance, reproducibility, and uniformity over the entire PEN substrate, highlighting the potential of this manufacturing technique in future low-cost, R2R fabrication of SWCNT computational devices.[68]

2.1.1.2 Flexible SWCNT analog and digital devices

SWCNTs provide a number of unique advantages over other semiconducting materials that are used for TFTs. Due to their sp^2 bonding and high carrier mobilities, SWCNT TFTs possess high drive current with long-term ambient stability. Moreover, their ultra-thin body and compatibility with common printing methods enable low-cost TFTs on flexible substrates with performance that is resilient to mechanical deformation. However, SWCNT TFT applications must still consider the effects of ink chemistry, network composition, and post-processing conditions in order to exploit these advantages. In particular, high-performance SWCNT TFTs on rigid substrates require carefully optimized device processing to reduce the effects of ambipolar transport and device-to-device variability. Key performance metrics for SWCNT TFT devices include ON/OFF ratio (typically greater than 10^3), carrier mobility (typically above 10 $cm^2V^{-1}s^{-1}$), and ON current (typically above 10 $\mu A \bullet \mu m^{-1}$). We refer the reader to the following comprehensive

reviews for further information on key device properties and requirements for printed[3] and high-performance[4] SWCNT TFTs.

Flexible smart devices require high-performance analog and digital components that can be fabricated on flexible substrates and properly operate under mechanical deformation.[4,8,10] Towards this end, several studies have established the performance and computational capabilities of flexible SWCNT devices through fabrication optimization. For further information on key device properties and requirements for SWCNT TFTs, we refer the reader to the following comprehensive review.[4] In a key demonstration of channel scalability, inkjet-printed SWCNT network channels have been used to fabricate R2R compatible transistors with channel lengths of 150-250 nm. These devices achieve ON/OFF ratios of ~10^3, transconductance (g_m) greater than 150 $\mu S \cdot \mu m^{-1}$, and a mobility as high as 209 $cm^2V^{-1}s^{-1}$.[69] Beyond traditional length scaling challenges, flexible SWCNT analog and digital electronics must demonstrate simultaneous computational complexity and minimal performance dependence on mechanical deformation. For example, SWCNTs have been used to fabricate capacitors, logic gates, and charge-trap floating gate memory units on flexible polyimide substrates using standard CMOS processing. These analog and digital devices use serpentine connections and neutral plane layouts to conformally laminate onto human skin with mechanical deformation (e.g., stretching, poking, and compression) leading to minimal performance variation.[70] In order to realize the full potential of possible deformation in flexible SWCNT electronics, s-SWCNT p-type devices are fabricated on a 1.4 μm poly(ethylene terephthalate) (PET) film using standard CMOS fabrication. These high-performance TFTs have been crumpled, bent down to ~40 μm radius of curvature, and compressively strained by 67% with negligible performance variation due to their ultrathin and

lightweight (3 $g \cdot m^{-2}$) nature. Similarly, fabricated p-type based logic gates maintain their functionality when compressively strained by 33%.[71]

While most flexible SWCNT devices have microsecond-scale stage delays and only use p-type TFTs, these two limitations can be overcome by using ultrahigh purity (>99.9%) s-SWCNT solutions and a scalable n-type doping process. To n-type dope s-SWCNT TFT devices, a thin 2 nm layer of Al is deposited on a bottom-gate/top-contact structure followed by a 40 nm Al_2O_3 encapsulation layer grown using ALD. The resulting n-type doping enables flexible devices with current densities over 17 $\mu A \cdot \mu m^{-1}$, ON/OFF ratios of ~10^6, and mobilities of ~50 $cm^2V^{-1}s^{-1}$. Additionally, flexible logic gates and ROs have been fabricated including a 5-stage RO with an oscillation frequency as high as 17.6 MHz,[72] demonstrating that state-of-the-art SWCNT devices on flexible substrates can achieve metrics that are competitive with SWCNT devices on conventional rigid substrates.

Beyond SWCNT TFTs and digital logic gates, other important functional components have been demonstrated, such as radiation-hard devices,[73,74] random number generators,[75] shift-registers, and tunable gain amplifiers.[15] In radiation-hard SWCNT devices, *in situ* and *in operando* total ionization dose (TID) effects have been measured for CMOS inverters fabricated using s-SWCNT random network channels, molecular dopants, and an Al_2O_3 encapsulation layer. While the n-type transistors were found to be the most TID-sensitive component, these inverters are TID-hard under dynamic bias operation.[73] Similarly, radiation-hard static random access memory (SRAM) cells fabricated using doping-free processing can function up to a 2.2 Mrad TID, establishing the capability of using SWCNT-based ICs in extreme environments.[74] In another study using a molecular doping and encapsulation method, a SWCNT SRAM cell has been

operated as a true random number generator through the digitization of random thermal noise. The generated bit output is confirmed to be random by established statistical tests for randomness, demonstrating the realization of a ubiquitous security primitive crucial to future SWCNT-based applications.[75] Using ultrahigh purity (99.997%) s-SWCNTs, a pseudo-CMOS circuit design, and state-of-the-art processing, low-voltage 8-stage shift registers operating at 50 kHz and tunable gain amplifiers with a gain of 1,000 at 20 kHz have also been fabricated,[15] showing the extensive functional capabilities of flexible SWCNT digital and analog devices.

2.1.1.3. SWCNTs in flexible display technologies

SWCNTs TFTs are expected to provide superior performance as drivers for display technologies due to their high current capacity, ultrathin size, optical transparency, and compatibility with scalable, low-temperature fabrication.[76] We briefly discuss a number of key demonstrations of the integration of SWCNT devices in flexible displays and refer the reader to the following comprehensive review on the fabrication, design, and integration of flexible smart display technologies.[77]

In one study, solution-based printing was used to create optically transparent SWCNT TFTs with stretchable electrodes and an elastomeric dielectric. These TFTs achieved high electrical performance that is retained at 50% strain and after 500 cycles at 20% strain, thereby allowing them to drive white organic light-emitting diode (OLEDs) at up to 30% strain.[78] However, practical display applications require the integration of TFT drivers in multi-pixel displays. Towards this end, SWCNT TFT drivers using polymer-sorted s-SWCNTs have been fabricated, showing an average mobility of 13 $cm^2V^{-1}s^{-1}$ and an ON/OFF ratio of over 10^6. These

high-performance SWCNT TFTs have been monolithically integrated with polymer-dispersed liquid crystals (PDLC) in an active matrix display, allowing a fully functioning seven-segment display to be achieved.[79]

In order to further confirm the uniformity and yield of SWCNT TFTs in larger displays, SWCNT TFT drivers have also been monolithically integrated in a flexible 64 × 64 pixel active-matrix OLED display (AMOLED). Through a heat pretreatment and cleaning process for the flexible PEN substrate, uniform display brightness and a high pixel yield (99.93%) are achieved. Over 8,000 characterized SWCNT TFTs show an average ON/OFF ratio of ~10^7 and a carrier mobility of 16 $cm^2V^{-1}s^{-1}$, with both metrics showing a standard deviation of less than 7% across the entire display.[80] Overall, these advances confirm the compatibility of SWCNT TFT drivers with flexible display technologies. SWCNT-based active-matrix electrochromic displays have also been realized,[81] validating the feasibility of integrating SWCNTs into a variety of display technologies.

2.1.1.4 SWCNTs in sensing technologies

Although SWCNTs have high chemical stability due to their stable sp^2 bonding, their high surface area makes them sensitive to non-covalent environmental interactions. More specifically, polar adsorbates result in charge redistribution within SWCNTs, affecting their charge transport properties. This principle is exploited when using SWCNTs as the active element for chemical and biological sensing, most commonly chemiresistive sensors and FET-based sensors. To further enhance sensing performance, SWCNTs are often functionalized to increase sensitivity, and multiplexed sensing is utilized for increased selectivity.[3] Early studies showed that these sensing

properties of SWCNTs could be exploited in molecular sensing applications,[13] driving the development of an entire field of research dedicated to the use of SWCNTs in large-scale, high-sensitivity sensors. We briefly discuss recent progress in SWCNT sensors, and refer the reader to the following comprehensive review of SWCNT-based sensor systems.[3]

Similar to their use as active-matrix drivers in display technologies, one application of SWCNTs for sensing technologies is as flexible active-matrix backplanes integrated with other sensing materials. In one demonstration, a 20 × 20 active-matrix was fabricated through R2R gravure printing using a flexible PET substrate, a s-SWCNT semiconducting channel, Ag nanoparticle ink electrodes, and a $BaTiO_3$ nanoparticle-based ink dielectric. The fabricated devices are a significant milestone in R2R printing due to their simultaneous high device yield above 98% and high resolution of 9.3 points per inch (ppi) along an entire 15 m PET roll. A pressure-sensitive rubber (PSR) film was then laminated on these devices in order to modulate their drain current when pressure is applied to the matrix, creating a functioning multi-touch pressure sensor.[82] This system shows negligible performance variations when bent down to a radius of curvature of ~1.85 cm.[83] In another study, a 16 × 16 active matrix using SWCNT TFTs and PSR pixels was fabricated through standard CMOS processing on a flexible polyimide substrate. The individual TFT devices achieved a high ON/OFF ratio of over 10^5, a high mobility of 17 $cm^2V^{-1}s^{-1}$, and nearly 99% yield over the entire 4-inch fabrication area. These devices achieve low-voltage operation with simultaneous fast response (< 30 ms) and high spatial resolution (~ 4 mm), and are capable of accurately sensing objects when bent down to a radius of curvature of 60 mm.[84] Overall, these advances present a path towards the realization of complex, large-area sensors, such as SWCNT-based “electronic skin” (e-skin) that is capable of mechanically conformal, multiplexed sensing.

For molecular sensing, FETs using single suspended SWCNTs have been characterized *in situ* when exposed to ionized gases. These devices show quantized and discrete increases in resistance due to SWCNT carrier depletion by single adsorption events of positive gas ions.[85] In another demonstration, a highly optimized fabrication strategy was employed to develop SWCNT-based H_2 sensors with sub-ppb detection. In particular, high-purity s-SWCNTs sorted by poly[9-(1-octylonoyl)-9H-carbazole-2,7-diyl] (PCz) were used to create a large semiconducting channel, which was then functionalized with Pd nanoparticles for the capture of H_2. A scalable, resistor-type fabrication design with Ti Schottky barrier contacts enabled detection of H_2 down to 890 ppb at room temperature and 89 ppb at 100 °C,[86] demonstrating that high-sensitivity sensors can be realized using high-throughput sensor fabrication methods.

Beyond molecular sensing, SWCNT-based humidity and temperature sensors have also been achieved. For example, SWCNT-based humidity sensors have been realized through the optimization of SWCNT CMOS FETs utilizing Pd (Sc) contacts for high-performance p-type (n-type) devices. These humidity sensors were fabricated on an ultrathin plastic foil that integrates a humidity-sensitive polymer variable resistor with a SWCNT three-stage CMOS RO functioning as a frequency-modulating signal processing unit. These devices consume minimal power (< 60 μW) and can be attached to human skin to detect relative humidity (RH) changes, such as the transition from dry (41% RH) to sweaty skin (84% RH).[87] Temperature sensors have also been fabricated using unsorted-SWCNT electrodes, high purity s-SWCNT channels, and a non-polar styrene-ethylene-butadiene-styrene (SEBS) film as both the substrate and dielectric. Most notably, different circuit configurations were explored, resulting in static differential and dynamic differential circuits for temperature sensing with sensitivities in the range of −20 $mV \cdot °C^{-1}$. Figure

2.1 shows a photograph of a temperature sensor conformally wrapped around a human wrist during bending and its stable temperature sensing operation when undergoing bending cycles. Overall, these temperature sensors achieve a low measurement error of ±1°C under uniaxial strain as high as 60%,[88] showing that SWCNT transistors can be used for both the analog and sensing electronics of complex environmental signals.

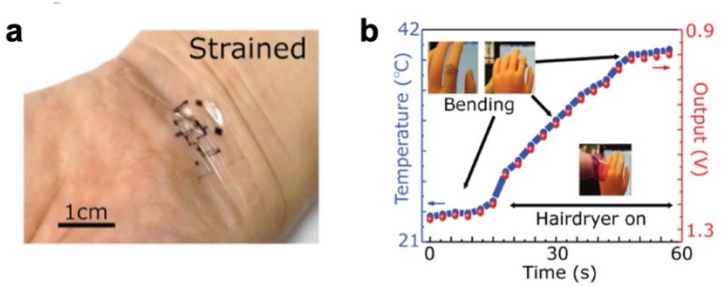

Figure 2.1 | Stretchable temperature sensing circuit. a, Optical photograph demonstrating skin-like conformity of a SWCNT sensor laminated onto a wrist during bending. **b,** Temperature sensor in stable operation during bending and heating while attached to a rubber prosthetic hand. Reprinted by permission from Springer Nature: Nature Electronics,[88] Copyright (2018).

In two other notable studies, time-based sensor interfaces[89] and transfer on biological surfaces[90] have been demonstrated. Briefly, time-based sensor interfaces enable robust, low-power sensing that can be readily integrated with traditional digital systems. Using 32 nm SWCNT technology (i.e., 32 nm minimum feature size), an integrated time-based IR sensor with a low supply voltage of 2 V has been shown to operate at ~100 kHz with a low power consumption of 130 nW.[89] In another study, the bio-integration capabilities of flexible SWCNT-based electronics were demonstrated by fabricating high-performance SWCNT devices on a transferable substrate. Through a sacrificial layer approach, these devices have been successfully transferred to several irregular biological surfaces including a human wrist, a biodegradable polymer, and a curved plant

leaf. The devices transferred onto the curved plant leaf exhibit low power consumption and high uniformity with negligible performance dependence on leaf curvature.[90] These two studies show the diversity of SWCNT-based sensor integration, highlighting the potential of SWCNTs in next-generation, energy efficient, conformable sensor systems.[91]

2.1.1.5 Integration of flexible SWCNT devices for smart systems

As covered in the previous sections, flexible SWCNT digital, analog, display, and sensor devices have been realized using scalable manufacturing methods. Therefore, monolithic integration of these components could provide a novel material platform for next-generation flexible smart devices.[2,5] Towards this end, a number of SWCNT-based integrated systems have been realized that exploit complementary sensing, computational, and manufacturing advantages. We briefly discuss recent progress in these integrated systems, and refer the reader to the following comprehensive review on SWCNT-based flexible electronic systems.[2]

Interactive, pressure-sensitive systems have been realized through the heterogeneous integration of multiple SWCNT electronic components. For instance, a user-interactive e-skin has been fabricated on a polyimide substrate by integrating a 16 × 16 SWCNT active-matrix with OLED/PSR pixels. The PSR increases in conductivity as pressure is applied to the active matrix, resulting in instantaneous pressure mapping through light emission and pressure magnitude feedback through the emitted light intensity.[92] In another example, fully-printed SWCNT TFTs have been integrated with a microcontroller and a Bluetooth communication chip to create a flexible environmental pressure sensor that is capable of wireless data transmission. Environmental pressure on the SWCNT TFT sensor modulates the transconductance by 48.1

$pS \cdot PSI^{-1}$ over a range of 0 – 42 PSI, such that this sensor is used as a flexible, low-cost tire pressure sensing system. This system has been further integrated with another material thickness sensing unit to create a smart tire sensor for real-time tire pressure and tread depth monitoring.[93]

Integrated systems capable of locally sensing bio-signals have also been explored. In one example, SWCNT TFTs are integrated with other materials to develop a flexible, printed healthcare wearable with UV, electrocardiogram (ECG), temperature, and acceleration sensors. The system uses a modular design such that the low-cost sensors applied directly to patient skin can be detached from the more expensive electronics components, allowing the wearable device to have both disposable and reusable components. As a proof of concept for practical use in healthcare, this sensor simultaneously monitored skin temperature, heart rate, UV exposure, and movement.[94] In another example, a wearable cardiac monitor was developed by integrating an ECG electrode, SWCNT electronics, and a color-tunable OLED (CTOLED). The weak ECG signal was amplified using SWCNT p-MOS inverters, allowing real-time display based on the voltage-dependence of the CTOLED color. Moreover, the performance of each component was minimally affected by stretching and bending, highlighting its potential as a practical wearable. Figure 2.2 shows a photograph of this cardiac monitoring system, as well as the CTOLED color change with normal and abnormal ECG readings.[95]

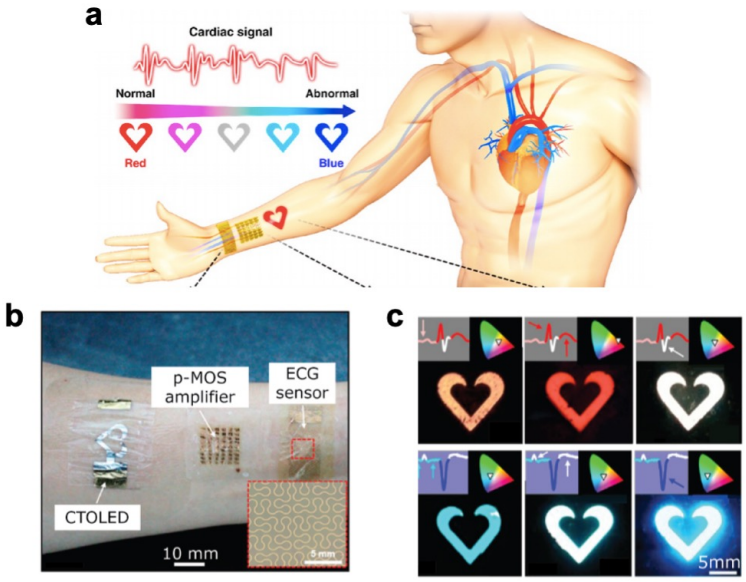

Figure 2.2 | Wearable cardiac monitoring system. a, Illustration of the wearable cardiac monitoring system. **b,** Photograph of the wearable system consisting of a stretchable electrode for ECG signal sensing, a SWCNT p-type FET amplifier for signal amplification, and color-tunable wearable OLED for real-time user feedback. **c,** OLED color changes synchronized with normal (right, top) and abnormal (right, bottom) ECG readings. Reprinted with permission from [95]. Copyright 2017 American Chemical Society.

A standalone flexible temperature sensing system has also been achieved by integrating a SWCNT CMOS voltage-controlled oscillator (VCO), a temperature sensing interface, a flexible antenna, and a flexible Li-ion battery into a single package. The SWCNT transistors were optimized through channel length scaling, contact selection, and the use of ultrahigh purity s-SWCNTs, enabling SWCNT CMOS VCOs with oscillation frequencies as high as 1.98 GHz. The integration of these VCOs with the other package components onto a flexible PET substrate then allowed for the realization of a standalone temperature sensor capable of transmitting temperature data. As the temperature changed from 65 to 90 °C, the antenna output frequency changed from 0.78 to 1.08 GHz, demonstrating sensing and data transmission at frequencies relevant for practical wireless communication.[96]

The examples outlined above highlight the potential of flexible SWCNT electronics in Internet of Things applications. In this context, SWCNT devices offer several distinct advantages including low-cost manufacturing, high electronic performance, and broad sensing capabilities. However, many SWCNT-based systems still rely on external Si electronics, highlighting the need for further development of SWCNT electronics capable of performing important functions such as signal processing, data storage, and communication.

2.1.2 Planar high-performance computing

2.1.2.1 Progress in processing of conventional SWCNT devices

Since the realization of the first SWCNT FET,[97] understanding and optimization of processing-property relationships has allowed substantial improvements in SWCNT FET metrics over the last two decades.[1,4,5] The key challenges to date include doping, controllable SWCNT assembly, solution-processing optimization, and wafer-scale uniformity. In this section, we discuss recent progress in processing of conventional SWCNT devices and advances in key challenge areas. For a comprehensive assessment of challenges and opportunities in SWCNT circuits we refer the reader to the following publications for further information.[3,98]

Most modern computing electronics rely on complementary FETs with controllable n-type and p-type doping. For SWCNTs, early work showed that despite strong p-type doping by atmospheric adsorbates (primarily adsorbed oxygen), selective carrier injection can be achieved through contact metal work function engineering. Pd[99] and low-work function metals (primarily Sc)[100] allow the creation of p-type and n-type SWCNT FETs, respectively. Despite challenges in the ambient stability of Sc contacts, this contact metal design is extensively used and enables

several advanced SWCNT CMOS ICs (see Section 2.1.2.2). Given that SWCNT p-type doping results from ambient exposure, alternative n-type doping strategies have been proposed. In one approach, the sensitivity of SWCNTs to molecular adsorbates is exploited to achieve n-type doping by using an electron-donating small molecule adsorbate. Tunability of this n-type doping is enabled by controlling the amount of time SWCNT channels are exposed to the molecular dopant (pentamethylrhodocene dimer), resulting in uniform n-type doping of SWCNT TFTs that are stable in ambient conditions for over one year.[101] Another strategy to induce n-type doping is dielectric interface engineering. In this case, SiN_x thin films deposited through plasma-enhanced chemical vapor deposition (PECVD) are used to encapsulate s-SWCNT network channels in TFTs. The Schottky barrier widths at the SWCNT/metal contact interface are reduced due to the fixed positive charges in the SiN_x films, resulting in n-type SWCNT TFTs by selective injection of electrons. These n-type SWCNT TFTs show mobilities of ~10 $cm^2V^{-1}s^{-1}$, high uniformity, and air stability for up to 30 days.[102] Similarly, tunable n-type electrostatic doping has been achieved using non-stoichiometric HfO_2 encapsulation. Fine-tuning of the SWCNT n-type doping is realized through optimization of the ALD oxide growth, with the ability to achieve unipolar n-type operation and threshold voltage control in s-SWCNT TFTs. This oxide doping scheme has also been confirmed to be compatible with work function metal doping strategies, allowing a dual doping strategy for SWCNT CMOS TFTs. This dual doping strategy has allowed the realization of highly symmetric n-type and p-type CMOS TFTs, with the resulting CMOS logic gates (i.e., NOT, NAND, and NOR) possessing high uniformity and performance metrics.[103]

Given that post-processing purification techniques have achieved the highest s-SWCNT enrichment purities, significant efforts have been made toward the selective placement of solution-

processed SWCNTs on target substrates. Early efforts in selective placement demonstrated s-SWCNT channels of percolating random networks and aligned films, while more recent efforts have focused on selective SWCNT placement with controllable pitch. For example, a substrate-agnostic method for selective, aligned self-assembly of SWCNTs has been realized via ion-exchange chemistry. In this approach, a surface monolayer of 4-(N-hydroxycarboxamido)-1-methylpyridinium iodide (NMPI) selectively assembles on HfO_2 trenches but not on the surrounding SiO_2, such that ion exchange between the NMPI and the SWCNTs wrapped in ionic surfactants (i.e., ion exchange between I^- in NMPI and Na^+ in sodium dodecylsulfate) causes strong Coulombic interactions. These interactions lead to selective and aligned placement where the pitch is controlled by altering the width of the functionalized HfO_2 trenches. However, placement yield significantly decreases at small trench widths, dropping from ~80% to below 10% at 150 nm and 70 nm trench widths, respectively.[104] A similar method for selective self-assembly has been developed based on polymer-wrapped s-SWCNTs using PFO-BPy. A self-assembled monolayer of long-chain aniline hydroxamic acid on a pre-patterned HfO_2/Al_2O_3 surface is utilized, enabling selective placement of polymer-wrapped SWCNTs on HfO_2 trenches through *in situ* diazotization of the aniline. High-performance SWCNT CMOS ROs with switching frequencies as high as 282 MHz have been fabricated in this manner using CMOS-compatible manufacturing processes, 100 nm channel lengths, and trenches with a 200 nm pitch.[105]

Beyond self-assembly, deposition of highly aligned SWCNT networks has also been achieved. For example, a solution-processed s-SWCNT network has been formed on a stretchable PMMA carrier film, which is then pressed on a stretched elastic polydimethylsiloxane (PDMS) film. The elastic PDMS film is subsequently relaxed such that the attached s-SWCNT network is

compressed along a single dimension, significantly increasing both the alignment and density of the network. By using a shrinking ratio of four, SWCNT random networks are aligned with an angular orientation standard deviation of 6.5° with network densities increased to 37 SWCNTs·μm^{-1}. These films can be transferred to target substrates, achieving full-surface coverage of dense, highly aligned s-SWCNT films for high-performance FETs.[106] This method is further enhanced through the use CVD-grown aligned SWCNTs. In this case, aligned SWCNTs are transferred to a carrier film, after which they are compressed by a factor of 10 along the direction perpendicular to alignment. This technique, referred to as density amplification, allows for a ten-fold increase in the original SWCNT density while retaining near-perfect alignment in millimeter-sized films. FETs fabricated using these films have attained record high performance for SWCNT FETs based on CVD-grown SWCNTs, further confirming the effectiveness of this method.[107]

While solution-processed s-SWCNTs are widely used in high-performance SWCNT FETs, the large parameter space for solution-processing methods (e.g., temperature, solvent, and surfactant concentrations) makes optimization challenging. Nevertheless, extensive studies have advanced the understanding of processing-property relationships for solution-based methods. In one study, high-performance SWCNT FETs have been achieved through the development of post-processing treatments to prevent performance degradation caused by solution-processing residues. Specifically, aligned films of PFO-BPy-wrapped SWCNTs deposited through floating evaporative self-assembly (FESA) have been post-processed through extensive solvent rinsing and high-vacuum annealing. These treatments were designed to remove chloroform residues and partially decompose polymer wrappers, resulting in FETs with a seven-fold improvement in their on-state conductance and current densities comparable to or exceeding those of conventional GaAs and Si

FETs.[108] In another demonstration, both FET performance enhancement and reduction in solution-processing costs were achieved through a recycling strategy for polymer-sorted SWCNT solutions. In particular, PCz-wrapped s-SWCNTs in toluene were filtered and washed by THF so that excess polymer was collected in the filtrate, achieving both the removal of polymeric residue from the sorted SWCNTs and the collection of expensive polymer material for recycling. The filtered SWCNTs were then redispersed in chloroform and used to fabricate FETs without further post-treatment. FETs fabricated using the treated SWCNTs showed a 20-fold contact resistance reduction and a 3-fold current density increase, further confirming the importance of residue removal in performance enhancement of solution-processed SWCNT films.[48]

A crucial prerequisite for commercialization of SWCNT devices is the realization of uniform wafer-scale fabrication. Therefore, research efforts have focused on the following challenges: wafer-scale deposition of SWCNT films and uniform FET fabrication using these films. Using dip coating, randomly oriented s-SWCNT networks have been achieved on a rigid 4-inch Si substrate. A total of 25,200 SWCNT FETs with various geometries were fabricated using standard CMOS processing, achieving nearly 100% yield and narrow distributions in key performance metrics (e.g., current density, ON/OFF ratio, threshold voltage, and mobility) over the entire substrate area.[109] To further test the wafer-scale compatibility of SWCNTs with complex fabrication designs, three-dimensional (3D) fin-structured SWCNT FETs were fabricated on a rigid 8-inch Si substrate. Full-surface coverage of the SWCNT networks, including coverage of the fin-structure sidewall, was achieved through surface functionalization using an amine-terminated adhesion layer (poly-L-lysine) and dip coating using a high purity s-SWCNT solution. The fabricated fin-structured SWCNT FETs show high processing uniformity, achieving a

significant milestone in the commercial compatibility of SWCNT electronic devices.[110] A related study also performed thorough characterization of wafer-scale TFTs fabricated using s-SWCNTs films. In this case, wafer-scale s-SWCNTs network films were deposited on 4-inch Si substrates and backplane glasses (370 mm × 470 mm) by dip coating in high-purity polymer-sorted SWCNT solutions. Detailed statistics were obtained using custom image processing software, which showed that the films are highly uniform throughout the 4-inch substrate, with coefficients of variance below 10%.[111]

2.1.2.2 Progress in conventional SWCNT integrated circuits

Progress in the performance of individual SWCNT FETs has enabled advances in state-of-the-art SWCNT ICs. As key processing steps (e.g., doping and channel deposition) have become more optimized and reproducible, SWCNTs ICs have achieved considerable performance improvements and important computational functions.[112] We briefly discuss recent progress in conventional SWCNT ICs, and refer the reader to the following publications for further information.[4,112]

Optimization using doping-free processes and ultrahigh purity (>99.9%) s-SWCNTs has enabled performance improvements in key metrics of SWCNT digital ICs. In one example, ultrahigh purity s-SWCNT networks were used to fabricate SWCNT FETs with high yield, performance, and uniformity. Specifically, Sc source and Pd drain contacts were used to create p-type and n-type FETs, respectively, in devices with channel lengths longer than individual SWCNTs. The scalability of this device processing scheme was demonstrated by fabricating logic gates (e.g., NOT, NAND, NOR, and XOR), 2-to-1 multiplexers, D-latches, T-flip-flops, and 4-bit

adders. Most notably, eight 4-bit full adders with 132 individual SWCNT FET devices were fabricated with 100% yield.[113] SWCNT FETs with channel lengths less than 200 nm were also fabricated using the aforementioned processing design, with an additional high-temperature sorting polymer removal step and the use of a 7.5 nm HfO_2 gate dielectric. These FETs achieved a record high transconductance of 0.46 $mS \cdot \mu m^{-1}$ and current density of 0.55 $mA \cdot \mu m^{-1}$ at a low supply voltage of 0.8 V, allowing the realization of five-stage ROs with record high frequencies up to 5.54 GHz.[114]

In addition to performance improvements in conventional digital ICs, several other important functions have also been realized. CMOS SWCNT FETs with stable operation, high uniformity, and appropriate CMOS metrics (e.g., symmetric threshold voltages) have been fabricated using high-purity s-SWCNTs, adsorbed atmospheric dopants, and robust encapsulation layers. These achievements have been thoroughly confirmed with detailed performance statistics on over 800 devices. Most notably, these statistics enabled the design, simulation, and large area fabrication of fully-functioning, energy-efficient static random-access memory (SRAM) cells.[115] In related work, a dual doping strategy (i.e., contact work function engineering and oxide electrostatic doping) was used to fabricate high performance CMOS SWCNT FETs with ~2.5 μm channel lengths. With these FETs, one of the most ubiquitous analog building blocks was achieved, namely an operational amplifier (op-amp). Two-stage op-amps were fabricated and achieved high gain, linearity, and temporal stability at supply voltages as low as 480 mV. On-chip integration with a SWCNT FET chemoresistive breath sensor was further demonstrated, highlighting the potential use of these op-amps as analog subsystems in mixed-signal ICs.[116] Figure 2.3 shows the

circuit schematic for this breath sensor integrated with an analog subsystem, as well as a false-colored SEM image of the fabricated device.

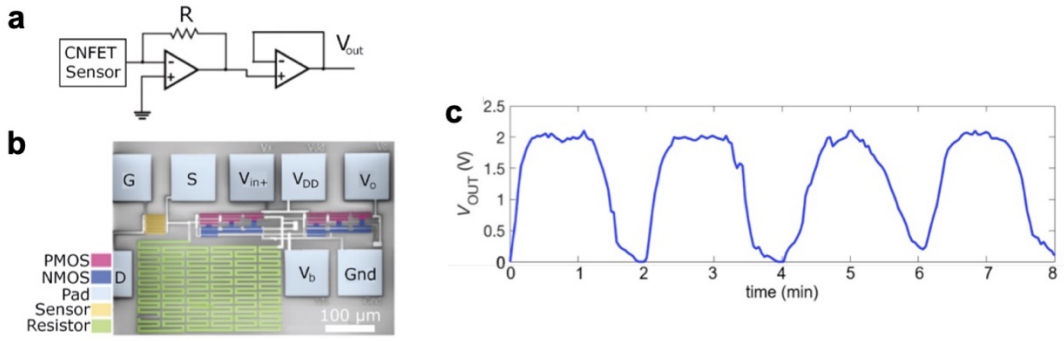

Figure 2.3 | Integrated breath sensor with an analog sub-system. a, Circuit schematic of the chemoresistive breath sensor with an analog SWCNT CMOS 2-stage op-amp. **b,** False-colored SEM image of a fabricated on-chip sensor-analog integrated system. **c,** Output of analog sub-system when sensor is exposed to alternating warm breaths and ambient N_2. © 2019 IEEE. Reprinted, with permission, from [116].

2.1.2.3 Scaling of conventional high-performance SWCNT FETs

The slowing of progress in Moore's Law scaling presents a unique opportunity for other semiconductor material systems to compete with Si in post-Moore computing systems. When compared to Si FETs, SWCNT FETs offer unique advantages in scaling for sub-10 nm channel length FETs including small size (~1 nm diameter), superior charge transport properties, and improved energy-delay product.[1] Despite the realization of complex digital ICs, such as a fully functional SWCNT computer,[117] SWCNT FETs must still overcome a number of length scaling challenges[118] in order to be truly competitive with established Si CMOS technology. We briefly discuss recent progress in scaling of conventional SWCNT FETs.

SWCNTs provide a number of unique advantages in high-performance digital FETs when compared with traditional Si devices. Due to their one-dimensional nature, SWCNTs allow for the

decoupling of vertical and lateral scaling while providing superior electrostatic control when used as semiconducting channels. Moreover, SWCNTs FETs attain high-performance with lower power consumption than traditional Si devices owing to their ballistic transport at relatively long channel lengths and their smaller intrinsic bandgap. However, high-performance digital applications using SWCNT must still overcome challenges to meet the requirements of metallic impurity levels below 1 ppb, controllable SWCNT placement with a uniform pitch (5 – 10 nm), and device performance variability. Monochiral enrichment is key to the latter requirement since the bandgap of a SWCNT is inversely proportional to its diameter, which implies that contact resistance, leakage current, subthreshold swing, and threshold voltage variability increase with increasing polydispersity. Key performance metrics for these devices include ON/OFF ratio (typically greater than 10^3), operating voltage (typically below 1 V), subthreshold swing (typically below 300 mV•decade^{-1}), and ON current (typically above 100 μA•μm^{-1}). For further information, we refer the reader to the following comprehensive review that highlights key requirements for high-performance digital SWCNT FETs.[1]

While different metrics of high-performance SWCNT FETs can be improved, the most prominent of these is the reduction of transistor channel length. More specifically, the development of SWCNT FETs with sub-10 nm channel lengths is of crucial importance since SWCNT FETs are expected to outperform traditional Si CMOS technology in this scaling limit.[1] The first sub-10 nm SWCNT FET was fabricated on a single SWCNT using various contacts to study channel length scaling from 320 nm to 9 nm. Characterization of the 9 nm p-type SWCNT FET showed a low operating voltage of 0.5 V with a subthreshold swing (94 mV·decade^{-1}) that was lower than theoretical predictions (~170 mV·decade^{-1}). Numerical device simulations predict that this FET

can outperform competing Si FETs, and highlights the need for further investigation of charge transport at the SWCNT-contact interface.[119] Both p-type and n-type SWCNT FETs were later demonstrated using processes compatible with very large scale integration (VLSI) design and channel lengths ranging from 90 nm to sub-20 nm. Fully functioning inverters with frequencies up to 1 MHz and an IR light sensor with a low power consumption of ~130 nW were realized using these devices. It is worth noting that while direct CVD growth of aligned SWCNTs was used to overcome potential misalignment issues, the low s-SWCNT purity necessitated electrical breakdown to remove the large number of m-SWCNT impurities present in the as-grown SWCNTs.[120] Further channel length scaling was achieved with the fabrication of top-gated SWCNT FETs with gate lengths as short as 5 nm. While Pd/Sc contacts showed nearly symmetric p-type/n-type transfer characteristics, the most notable performance improvements were achieved using graphene contacts including a low supply voltage of 0.4 V and a small subthreshold slope of 73 $mV \cdot decade^{-1}$. Figure 2.4 shows a cross-sectional transmission electron microscope (TEM) image of a 5 nm SWCNT FET device as well as the transfer characteristics of three representative 5 nm devices. Direct comparison further confirms that SWCNT FETs outperform Si FETs at the sub-10 nm channel length scale, most notably in the energy-delay product. Additionally, this fabrication scheme has been utilized to fabricate CMOS inverters with a pitch size as small as 240 nm.[16] While these advances highlight the potential of SWCNT FETs in aggressively scaled digital technologies, a deeper understanding of how channel length scaling affects other performance metrics (e.g., early device degradation)[121] is needed.

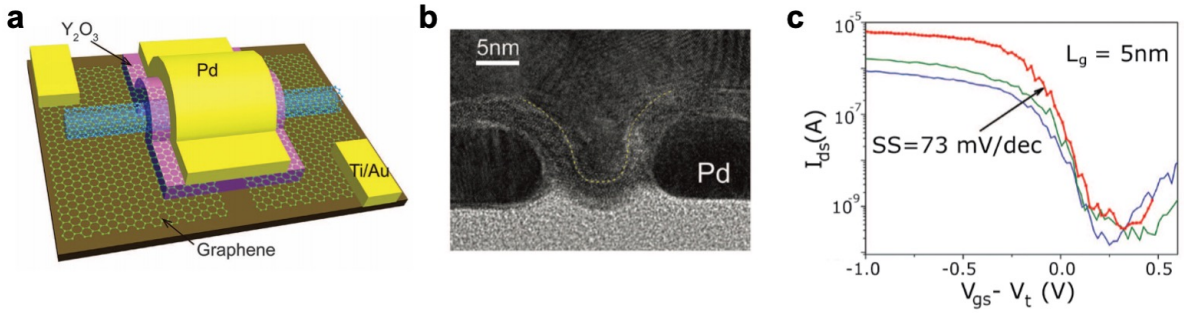

Figure 2.4 | SWCNT FET scaled down to a 5 nm gate. a, Schematic showing device design for graphene-contacted SWCNT FET. **b,** Cross-sectional TEM image of a 5 nm gate length SWCNT FET with Pd contacts. **c,** Transfer characteristic of three representative 5 nm gate length SWCNT FETs. From [16]. Reprinted with permission from AAAS.

Scaling requires both high performance semiconducting channels and low resistance contacts at short length scales. While these studies demonstrate that SWCNTs can be used in channels as short as 5 nm, the absolute values of contact resistance significantly increase at contact lengths below 100 nm.[118] To overcome this limitation, a strategy for fabricating end-bonded contacts to SWCNTs has been developed. End-bonded contacts exhibit superior length-scaling performance in addition to avoiding potential SWCNT-contact coupling issues present in conventional side-bonded contacts. End-bonded contacts have been fabricated by depositing Mo contacts on SWCNTs and annealing up to 850°C in vacuum. These conditions result in the diffusion of carbon atoms from the partially covered SWCNT into the Mo contact, resulting in strong carbide bonds between the SWCNT and Mo contact. This strategy achieves essentially barrier-free contacts with length-independent contact resistance from 300 nm down to 9 nm contact length.[122] Further optimization of side-bonded contacts has been realized through the fabrication and study of contact resistances from 232 individual SWCNT FETs. This study showed that a 10 nm contact length achieves a contact resistance as low as 6.5 kΩ per contact, although the median

contact resistance is significantly higher (18.2 kΩ per contact). This large variation in contact resistance is found to become significant at sub-20 nm contact lengths. These results also showed that the large variations in contact resistance at these contact lengths are independent of SWCNT diameter, highlighting the need for further understanding the origin of contact resistance variations.[123] As an alternative approach, n-doped graphene source contacts have been used in SWCNT FETs with sub-15 nm channel lengths. This so-called "Dirac-source" FET achieves an average subthreshold swing of 40 $mV \cdot decade^{-1}$ at room temperature due to the narrow electron density distribution around the Fermi level of the graphene contact. This work represents a significant advance since it provides a path towards simultaneous contact length scaling and increased energy efficiency.[124]

Apart from length scaling of individual FET components, length scaling of the entire device footprint is needed, which includes the channel, contact, and spacer lengths. While footprint scaling presents a considerable challenge, advances in contact length scaling has enabled SWCNT FETs with footprints that surpass leading Si technologies. In one such example, p-type SWCNT FETs were fabricated with gate lengths as short as 11 nm and total lateral footprints down to 40 nm. These devices were demonstrated using both individual and arrays of s-SWCNTs, where individual s-SWCNT devices showed a pitch-normalized current density of ~0.9 $mA \cdot \mu m^{-1}$ and a subthreshold swing of 85 $mV \cdot decade^{-1}$ at a low supply voltage of 0.5 V. While individual s-SWCNT devices present a substantial performance improvement when benchmarked with competing Si FETs, performance results are mixed for s-SWCNTs array devices. Compared to Si FETs, s-SWCNT array devices are able to deliver higher ON-state currents at half the supply voltage, but suffer from a relatively low yield of ~30% and a poor subthreshold swing of ~500

mV·decade^{-1}.[125] Another study highlighted the potential performance improvements of SWCNT FETs through the use of a back-gate geometry. The benefits of back-gate geometries in aggressively scaled, VLSI compatible SWCNT FETs were rigorously quantified, including SWCNT inverters with a gate length and contacted gate pitch of 9 nm and 30 nm, respectively. Experimental data and simulations showed that when compared with other geometries (e.g., top-gated or gate-all-around), back-gated transistors showed a reduction in the energy-delay product by a factor of up to 2.8 due to a reduction in parasitic capacitances. These results confirmed the potential benefits of SWCNT FETs at nodes as small as 3 nm. [126]

Due to the small size and ballistic charge transport of aggressively scaled SWCNT FETs, important performance metrics become highly sensitive to processing with substantial device-to-device variation. In an effort to understand the effects of processing on threshold voltage variability, variable-temperature measurements and gate oxide thickness scaling studies have been performed using SWCNT FETs with channel lengths as short as ~20 nm. Experimental results for threshold voltage variability due to SWCNT diameter distributions showed a standard deviation of ~260 mV despite the fact that theoretical calculations predicted a standard deviation of 88 mV, which suggests another predominant source of threshold voltage variability. This predominant source was confirmed to be the random variation of fixed charges close to the oxide-SWCNT interface, suggesting that further gate oxide scaling could improve threshold voltage uniformity.[127] The effects of random charges at the gate oxide interface have been further studied, while a combination of experimental and simulated results revealed that they are also a major limiting factor in subthreshold swing performance.[128] Gate oxide scaling has been found to also reduce the effects of interface traps, resulting in nearly-hysteresis-free SWCNT FETs. For example, a gate

oxide with an effective thickness down to 1.6 nm was fabricated using e-beam evaporated TiO_2, which reduced hysteresis to less than 0.5% of the gate-source voltage range. Despite this achievement, these devices again exhibited large threshold voltage and subthreshold swing variations that could not be solely explained by differences in SWCNT diameters.[129] Overall, these results highlight the need for further study of robust dielectric engineering methods in order to achieve high-performance SWCNT FETs with concurrently high uniformity and reproducibility.

2.1.3 Three-dimensional monolithic logic-memory integration

One of the major challenges in current computing technologies is the separation of stored data from computational elements. The hierarchy of volatile and non-volatile memory requires the movement of large amounts data within different storage and computational units, leading to increased latency and energy consumption. The advent of non-volatile memory components (e.g., floating-gate memory, phase-change memory, and resistive random access memory) with small thicknesses and low-temperature fabrication makes three-dimensional (3D) logic-memory integration possible.[130] 3D integration with traditional rigid semiconductors has limited placement of the logic components to the substrate layer. However, the use of ultrathin logic components compatible with low-temperature processing facilitates 3D integration with arbitrary layering, reducing logic-memory spatial distances and increasing the effective available footprint. Since SWCNTs exhibit high electronic performance and meet all the requirements for 3D integration, they have enabled advanced 3D monolithic logic-memory integration applications. In this section,

we introduce recent progress in monolithic 3D integration of logic and memory based on SWCNT devices.

Monolithic 3D integration of Si CMOS and SWCNT FETs has been demonstrated using VLSI-compatible, low-temperature (< 180 °C) fabrication. Following standard Si CMOS fabrication on a rigid Si substrate, an interlayer dielectric is deposited to allow for the fabrication of SWCNT FETs while connections to the underlying Si CMOS FETs are provided using high-density interlayer vias. Gate-level and circuit-level integration have been achieved using both SWCNT and Si FETs with a fixed channel length of 1 μm, demonstrating hybrid Si-SWCNT digital logic integration.[131] Si FETs, SWCNT FETs, and non-volatile metal-oxide resistive random-access memory (RRAM) have also been integrated in 3D using a similar fabrication process with a maximum processing temperature of 200 °C. The fabricated structure is composed of four vertically-stacked layers (1st: Si logic; 2nd and 3rd: RRAM; 4th: SWCNT logic), where logic and memory components between any two layers can be interconnected.[132] While this 3D monolithic integration design is incompatible with a number of semiconductors (e.g., III-V compound semiconductors) due to their high processing temperatures, a new processing paradigm ("X3D") has demonstrated successful heterogeneous integration of Si, III-V compound semiconductors, and SWCNT technologies on a single chip. An identical process flow is used to fabricate five vertically stacked layers with different semiconductor technologies including Si junction-less nanowire FETs (JNFETs), III-V JNFETs, and SWCNT FETs. This X3D integration paradigm is enabled by the high-temperature synthesis of the semiconducting material on a donor substrate, release of this material in solution, solution-based deposition on the integration layer, and subsequent low-temperature fabrication. Similar to previous demonstrations, digital logic

circuits have been fabricated using different semiconductor technologies, highlighting the high level of integration that can be achieved using the X3D processing paradigm.[133]

By integrating diverse functional components, nanosystems with complex computational and sensing capabilities have been realized. In one of the most complex nanoelectronic systems demonstrated to date, the 3D monolithic integration of one million RRAM cells, two million SWCNT FETs, and high-performance Si CMOS logic has recently been achieved. This integrated system is capable of sensing and classifying ambient gases by capturing massive amounts of sensing data, storing this data, and then performing on-chip processing, resulting in a highly processed output. The nanosystem is composed of four vertically stacked layers with five integrated subsystems including a SWCNT-based classification accelerator, RRAM non-volatile memory, SWCNT-based row decoders for accessing memory, SWCNT FET functionalized vapor sensors, and Si interface circuits (e.g., amplifiers and multiplexers). Figure 2.5 shows a diagram of the 3D nanosystem architecture, as well as a cross-sectional TEM image of the fabricated structure. This large-scale integration is enabled by dense back-end-of-line interlayer metal wire vias, which can reach vertical connectivity densities that are 1,000 times higher than conventional methods.[134] Additionally, 3D monolithic integration has been applied to an unconventional system architecture by employing SWCNT FETs and RRAM memory to fabricate an end-to-end hyper-dimensional computing nanosystem. In this case, SWCNT FET and RRAM device variations are used to facilitate random projection operations, thus achieving high classification performance despite having 78% of its bits fixed in a single binary state. This brain-inspired nanosystem performs pairwise classification of 21 European languages on over 20,000 sentences with an average accuracy of 98%. When compared to Si CMOS implementations, projections show that

3D integration of hyper-dimensional computing can improve energy efficiency and reduce device footprint by a factor of 35 and 3, respectively.[135]

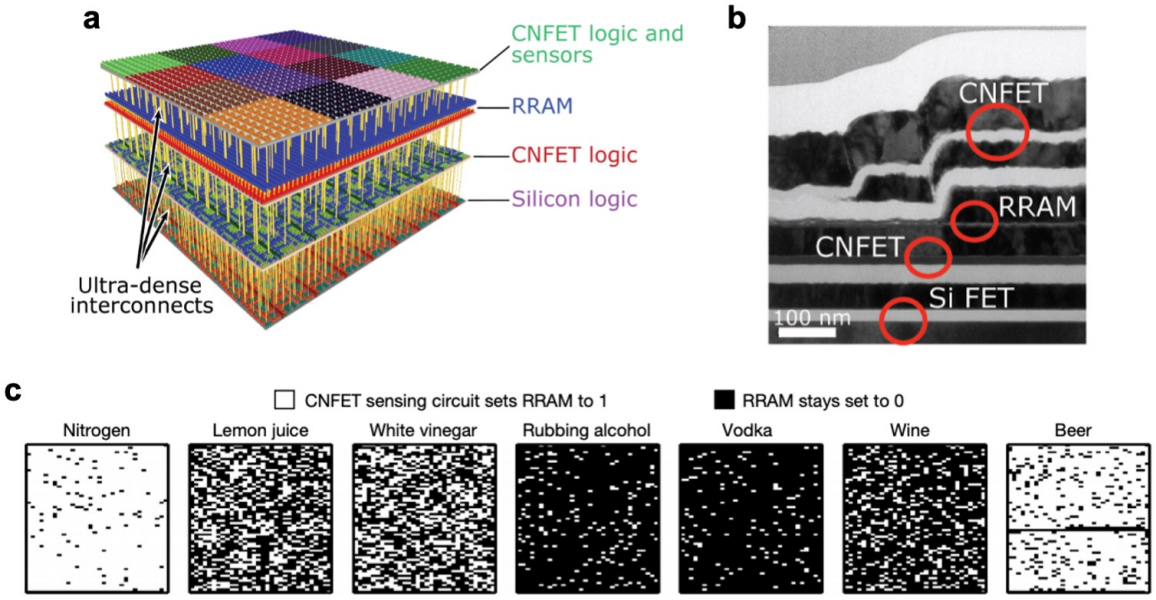

Figure 2.5 | 3D monolithic integrated system. a, Diagram of 3D monolithic integration of SWCNT FET-based sensors and logic, with traditional RRAM memory and Si devices. **b,** Cross-sectional TEM image of the fabricated integrated structure. **c,** Sensory data written to RRAM layer for seven ambient gases. Reprinted by permission from Springer Nature: Nature,[134] Copyright (2017).

2.1.4 Neuromorphic computing

Most computing systems today rely on multiple central processing units that are physically removed from memory components that store most of the processed data. This traditional computing architecture, known as the von Neumann architecture, has proven to be a robust generalized computing platform, but intrinsically suffers from memory-related constraints when processing large amounts of data. Overcoming this bottleneck of von Neumann computing has become increasingly important with the advent of artificial learning paradigms that often require

efficient parallel processing of massive data streams. Consequently, significant recent research has been devoted to alternative computing architectures that can achieve efficient distributed computation with co-localized computation and data storage.[136] In particular, neuromorphic architectures have emerged as a leading candidate for beyond-von-Neumann computing by imitating biological neural systems in order to achieve efficient computation.[137] Using established knowledge from the extensive study of SWCNT-based electronics, a number of SWCNT-based neuromorphic computing designs have been explored. In this section, we discuss recent progress in neuromorphic computing using SWCNT-based devices. For a comprehensive review of information processing in neuromorphic systems, we refer the reader to the following publication.[136]

Printed dual-gated SWCNT TFTs with electrolyte dielectric films have been pursued as artificial synapses. Specifically, synapse functionality is mimicked by using the gate electrodes as presynaptic inputs, while the drain-source current provides excitatory post-synaptic current (EPSC). Gate voltage spikes are applied, inducing the field-driven migration of protons in the electrolyte dielectric film. When protons gather near the SWCNTs, the channel is depleted and exhibits a high resistance, enabling short-term plasticity due to the slow proton relaxation process. A range of synaptic behaviors have been demonstrated, most notably controllable paired-pulse facilitation through changes to the gate voltage spike width and interval.[138] Another synaptic transistor has been explored using a thin Au floating gate layer inside the gate oxide of SWCNT FETs. The duration and amplitude of gate voltage pulses (i.e., presynaptic spikes) adjust the charge stored in the floating gate, enabling precise modulation of the channel current (i.e., postsynaptic current). In this manner, the synaptic transistor shows adjustable weight update linearity and

variation margin. Beyond single device functionality, a system-level framework has been designed and simulated using a simplified spike-timing-dependent plasticity (STDP) scheme based on crossbar hardware architecture. Unsupervised learning on the MNIST database has been simulated, showing that the large weight variation margin significantly enhances pattern recognition accuracy.[139]

SWCNT synaptic transistors have also been fabricated on wafer-scale aligned SWCNTs to further improve performance. These devices show repeatable gate oxide charge trapping and large ON/OFF ratios, resulting in robust synaptic operation with controllable channel conductance and large dynamic range (i.e., over one order of magnitude in conductance modulation). Additionally, potentiation/depression synaptic behavior has been achieved with high cycling stability and long-term retention. Figure 2.6 shows a schematic of the implemented spiking neural network, as well as how the pattern recognition rate on the MNIST database changes with increasing training epochs and output neurons. Further simulations have studied the learning tradeoffs of different synaptic characteristics, noting that although an abrupt conductance modulation strategy increases initial recognition rate of the neural network, excessive abruptness causes premature saturation in recognition rate and limits overall performance.[17] A related three-terminal synaptic device was demonstrated by embedding a thin TiO_2 charge storage layer within the gate oxide. This synaptic resistor ("synstor") is fabricated as a three-terminal transistor device with Schottky Al drain/source (input/output) contacts, but effectively functions as a two-terminal device since the gate electrode is simply used as the reference ground. Synstor conductance is modulated by applying equal voltage pulses at the input and output electrodes, demonstrating long-term (~10 years) nonvolatile memory and compatibility with concurrent inference-learning algorithms. This compatibility was

further confirmed by fabricating a 4 × 2 crossbar circuit using 72 synstor and 2 integrate-and-fire neuron circuits. Notably, this system shows a computational efficiency of ~1.6×10^{17} FLOPS·W^{-1} that surpasses state-of-the-art supercomputers,[140] thus highlighting the potential of SWCNT electronics for next-generation neuromorphic hardware compared to other emerging materials (e.g., MoS_2, perovskites, chalcogenides).[137]

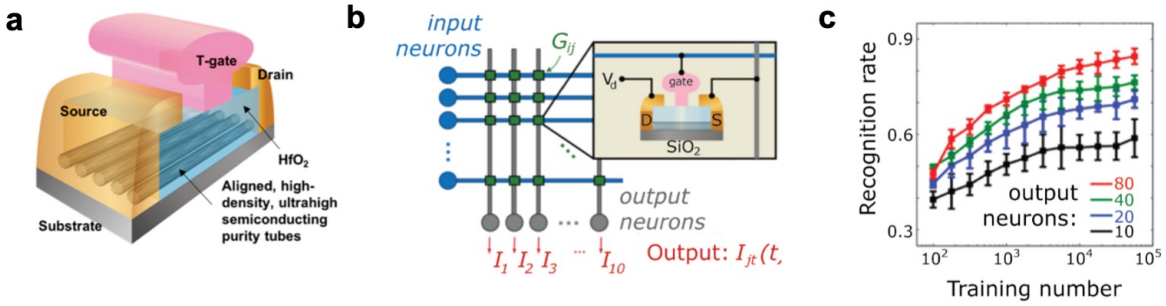

Figure 2.6 | SWCNT synaptic transistors for neuromorphic computing. a, Schematic of SWCNT FET synaptic transistor, showing aligned SWCNTs, a high-k dielectric gate, and T-gate electrode structure. **b,** Schematic of a neural network based on SWCNT FET synaptic transistors for unsupervised learning applications. **c,** Recognition rate results of MNIST data set number recognition using a simulated neural network with increasing number of neurons. Reprinted with permission from [17]. Copyright 2018 American Chemical Society.

2.2. Electronic applications of chirality-enriched SWCNTs

2.2.1 Charge transport in FETs

Initial demonstrations of SWCNT FETs and SWCNT-based electronics suffered from poor charge transport performance due to inadequate SWCNT placement control and high levels of metallic impurities.[9] The advent of improved SWCNT placement and post-processing purification methods for SWCNT electronic-type enrichment (most often semiconducting enrichment)[8]

resulted in demonstrations of SWCNT-based electronic devices with complex computational functionality (see Section 2.1). However, electronic-type enriched solutions commonly have large chiral polydispersities with SWCNT diameters in the range of 0.8 – 1.7 nm, which results in bandgap distributions in range of 0.5 – 1 eV. Since Schottky barrier control is critical in SWCNT FET charge transport, changes in SWCNT bandgap lead to changes in contact behavior (i.e., Ohmic versus Schottky) that affect on-state resistance, charge injection and threshold voltage. SWCNT FET charge transport is carried through an ensemble of SWCNTs, such that large chiral polydispersity leads to broad distributions of individual SWCNT metrics and results in large device-to-device variability.[1] For this reason, improved chirality monodispersity within the semiconducting SWCNT channel leads to favorable improvements in FET performance. In this section, we introduce recent progress towards monochiral SWCNT FETs and the effects of chiral distributions on SWCNT charge transport.

In order to study the effect of chiral polydispersity on the charge transport of s-SWCNT networks, dispersions have been prepared using various SWCNT sources (e.g., CoMoCat, HiPco, and tailored blends) and conjugated polymers (e.g., PFO and F8BT).[141] Notably, the tailored blend was designed to provide a large difference in SWCNT bandgaps by using majority (7,5) large-bandgap SWCNTs and minority (10,5) small-bandgap SWCNTs. As shown in Figure 2.7, the tailored blend devices showed 20-25 times lower ON current and reduced carrier mobilities when compared to HiPco-based (i.e., large chiral polydispersity) devices. These results were further elaborated by photoluminescence (PL) and electroluminescence (EL) characterization of optical emission in the channel, which revealed preferential charge transport through the smaller bandgap semiconducting SWCNTs despite them only making up a small fraction of the SWCNT network.

These results show the benefits of reducing SWCNT diameter polydispersity for improving charge transport performance. Similar follow-up studies have established the temperature-dependent[142] and inter-tube[143] charge transport properties of mixed-chirality s-SWCNT networks. Briefly, experimental and simulated charge transport studies suggest that monochiral, large-diameter (>1.2 nm) SWCNT networks should have the lowest contact resistance, highest mobility, and lowest temperature dependence when compared with other SWCNT networks. These studies provide rational network design guidelines for the optimization of chirality-enriched SWCNT FETs.

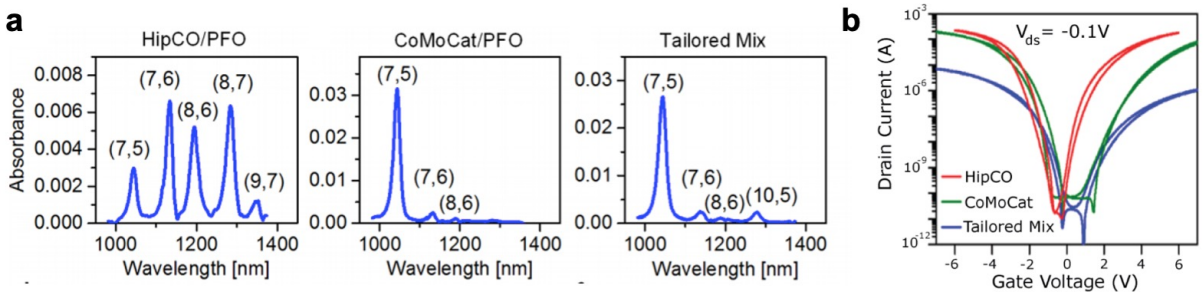

Figure 2.7 | Charged transport of mixed SWCNT networks. a, Absorbance spectra of three polymer-sorted s-SWCNT dispersions with different SWCNT chiral distributions. **b,** Transfer characteristic of mixed networks in SWCNT FETs. A tailored mixed network consisting primarily of (7,5) and (10,5) SWCNTs shows decreased performance, demonstrating the impact of diameter distribution on mixed network charge transport. Reprinted with permission from [141] (link: https://doi.org/10.1021/acsami.6b00074). Copyright 2018 American Chemical Society. Further permissions related to this material should be directed to the American Chemical Society.

SWCNT FETs with nearly monochiral s-SWCNT channels have also been demonstrated including FETs based on PFO-BPy-wrapped (6,5)[144] and ATPE-separated (9,8) SWCNTs.[145] Both of these reports show high single-chirality abundance in their SWCNT solutions, enabling the fabrication of SWCNT network FETs with mobilities between 2-4 $cm^2V^{-1}s^{-1}$. SWCNT FETs using channels of aligned ATPE-separated (6,5) SWCNTs have also been demonstrated using a wafer-

scale vacuum filtration alignment technique, although these devices exhibit low ON/OFF ratios due to SWCNT-SWCNT screening effects.[146] Solution-processed monochiral SWCNTs are also compatible with additive manufacturing techniques. Aerosol jet printed devices using PFO-BPy-wrapped (6,5) SWCNTs have been fabricated in both traditional FET[147] and unconventional vertical electrolyte-gated transistor (VEGT) designs,[148] demonstrating high reproducibility, ON-state conductance, and ON/OFF ratios. While most of these FETs have shown ambipolar charge transport, n-type and p-type doping of (6,5) SWCNT networks has been achieved through the use of 1,2,4,5-tetrakis(tetramethylguanidino) benzene (ttmgb) and molybdenum tris(1-(trifluoroacetyl)-2-(trifluoromethyl)ethane-1,2-dithiolene) ($Mo(tfdCOCF_3)_3$), respectively, enabling the fabrication of complementary inverters with high voltage gain (up to 52), rail-to-rail operation, and low power dissipation (45 nW).[149]

2.2.2 Optical emitters

High-speed information networks have enabled unprecedented advances in modern communication, with much of the existing infrastructure utilizing photonic systems and light as the carrier of information. Future communication systems based on classical and non-classical light sources will benefit from the development of robust, nanoscale, solid-state light sources with room temperature operation.[11,18] Towards this end, SWCNTs are a promising material platform for solid-state optical emitters due to their direct bandgap, small footprint, compatibility with modern fabrication technologies, emission tunability through chirality selection, and room-temperature exciton emission due to large exciton binding energies. However, since SWCNT optical emission depends on chirality, ideal SWCNT light sources should approach the monochiral

limit.[10,11] In this section, we discuss recent progress in the use of SWCNTs as classical and non-classical light sources.

2.2.2.1 Electrically-driven SWCNT optical emitters

Although SWCNT light emission is often demonstrated using optical pumping, electrically-driven light sources are preferred in applications where small device footprint, high-speed, and precise timing control are important. One-dimensional confinement enables Coulombic interactions such that, even at room temperature, localized excitons with large binding energies dominate SWCNT optical properties. Since excitons have wavefunctions that spatially extend outside of the nanotube, these excitons are sensitive to their local environment and spectral diffusion. Moreover, exciton diffusion along the length of SWCNTs leads to quenching by non-radiative decay processes (e.g., phonons, defects) resulting in low PL quantum yields on the order of ~1%. In addition to PL, EL can be achieved in ambipolar SWCNTs devices by simultaneous injection of electron and hole carriers at opposite contacts. Electron-hole recombination will take place in the SWCNT, leading to EL through radiative recombination where the emitted light is polarized along the SWCNT axis with its energy dependent on the chirality of the SWCNT. Unipolar devices at high driving voltages can also achieve light emission through impact ionization by "hot" carriers that generate electron-hole pairs for radiative recombination. For further information, we refer the reader to the following comprehensive review that discusses SWCNT electroluminescence phenomena.[150] With this motivation, several groups have demonstrated the feasibility of electrically-driven, monochiral SWCNT light emitters in a diverse range of

applications including polarized light emission,[81] narrow linewidth emission,[151] voltage-controlled trion emission,[152] and near-infrared (near-IR) OLEDs.[153]

To achieve narrow linewidth and polarized light emission, multiple studies have explored unique device architectures and SWCNT assembly. For example, individual air-suspended SWCNTs have been grown on a split-gate architecture to reduce spectral broadening. In this case, characterization of E_{11} emission from (12,4) SWCNT devices shows EL linewidths as narrow as 8 meV, highlighting the importance of heating effects, applied voltage biases, and the dielectric environment.[151] In another approach, aligned arrays of (6,5) SWCNTs were used to fabricate on-chip polarized light emitters. Evaporation-induced self-assembly was used for large-area fabrication of these devices, with an individual device channel area of 4 x 10 μm^2. Electrically-driven, linearly polarized emitters with an average degree of polarization of 78.5% were achieved despite linewidth broadening due to dark exciton and trion emission.[81]

Other studies have focused on applications using electrically-driven monochiral SWCNTs emitters. At high charge carrier densities, excitons may bound to an additional electron or hole, resulting in a charged three-body quasiparticle (i.e., a trion) that can emit light at lower energies. In order to demonstrate the potential impact of electrically-driven trion emission, electrolyte-gated transistors using copolymer-sorted (6,5), (7,5), and (10,5) SWCNTs have been fabricated.[152] EL and PL characterization shows tunable trion emission at telecom wavelengths with linewidths less than 70 nm. Notably, high trion/exciton emission ratios are achieved at room temperature with low-voltage operation (< 3 V) and 67% degree of polarization through SWCNT alignment in (10,5)-based devices. In another application, the first SWCNT-based OLED emitters were achieved.[153] Specifically, PFO-BPy-wrapped (6,5) SWCNTs were embedded as active emitters in

an optimized OLED stack architecture with charge-blocking and doped charge transport layers. This OLED shows narrow linewidth (< 50 nm) emission near the 1,010 nm excitonic peak, highlighting the possibility of using SWCNTs to extend OLED emission into the near-IR regime.

2.2.2.2 SWCNT single-photon emitters

The single-photon emitter (SPE) is a fundamental component in emerging communication technologies, such as quantum information processing and quantum computing. Although SPEs have been realized in other material platforms, they are generally limited by cryogenic operation or emission outside of telecom wavelengths.[18] Early work on the optical properties of SWCNTs demonstrated desirable properties for single-photon emission, such as photon anti-bunching and emission wavelength tunability through chirality selection.[11,154] An ideal SPE requires a two-level system that emits identical photons one at a time. Although pristine SWCNTs generally fail to meet this criterion, the introduction of sidewall defects enables SWCNT single-photon emission. The resulting deep-level traps enable room-temperature exciton localization at defect sites, resulting in red-shifted defect emission (E_{11}*) with enhanced quantum yield and longer decay lifetimes.[11,18]

An early demonstration of SPE sidewall defects in SWCNTs was oxygen dopant states in (6,5) SWCNTs. Low-temperature PL and simulations of this defect system confirmed the key requirements for single-photon emission by providing strong evidence for the creation of deep trap states at the defect sites and exciton localization at these states.[155] Fluctuation-free, room-temperature, single-photon emission in the telecom range has been achieved using isolated oxygen dopant states introduced during electron-beam deposition of an SiO_2 encapsulation layer. PL

lifetimes in these functionalized SWCNTs were found to increase by an order of magnitude at room temperature. Photon antibunching of $g^{(2)}(0) < 0.1$ below 230 K and 0.32 at room temperature was also observed.[156] While these results highlight the potential of using the oxygen-doped SWCNT system for indistinguishable single-photon generation, challenges remain due to the high sensitivity of these defects to the local dielectric environment.[18,155]

As an alternative defect system, sp^3 states introduced via aryl sidewall functionalization offer unique advantages including relatively low sensitivity to their functional group chemistry and dielectric environment.[157] Initial studies of the PL decay dynamics of this system revealed a PL lifetime increase by a factor of 5-10. PL decay times were found to range from 77 ps for (7,5) SWCNTs to more than 600 ps for (5,4) SWCNTs, indicating that chirality control is necessary for most SPE applications.[158] Similarly, high-performance SPE was demonstrated using covalent sp^3 defects by reaction of aryl diazonium with (6,5), (7,5), and (10,3) SWCNTs encapsulated in surfactant or copolymer. As shown in Figure 2.8, aryl chemistry and SWCNT chirality selection were used to achieve room-temperature single-photon emission tuning across the most important telecom wavelengths including the O (1.3 μm) and C band (1.55 μm). Single-photon, shot-noise-limited emission with high rates and single-photon purity was achieved. Most notably, simultaneous room-temperature operation and high single-photon purities at high pump power excitation showed performance comparable to conventional solid-state SPEs.[159] Coupling between 2D photonic crystal microcavities and (6,5) SWCNT sp^3 defect state emission has also been used to fabricate high purity SPE with emission enhancement by a factor of ~50 and emission rates as high as $\sim 1.7 \times 10^7$ Hz.[160] Although the scalability of most defect-based SWCNT SPE systems remains largely unexplored, it has been found that sp^3 defects sites in ultrashort nanotubes (~40

nm length) dramatically increase their photoluminescence, suggesting their potential in highly-scaled photonic systems.[7]

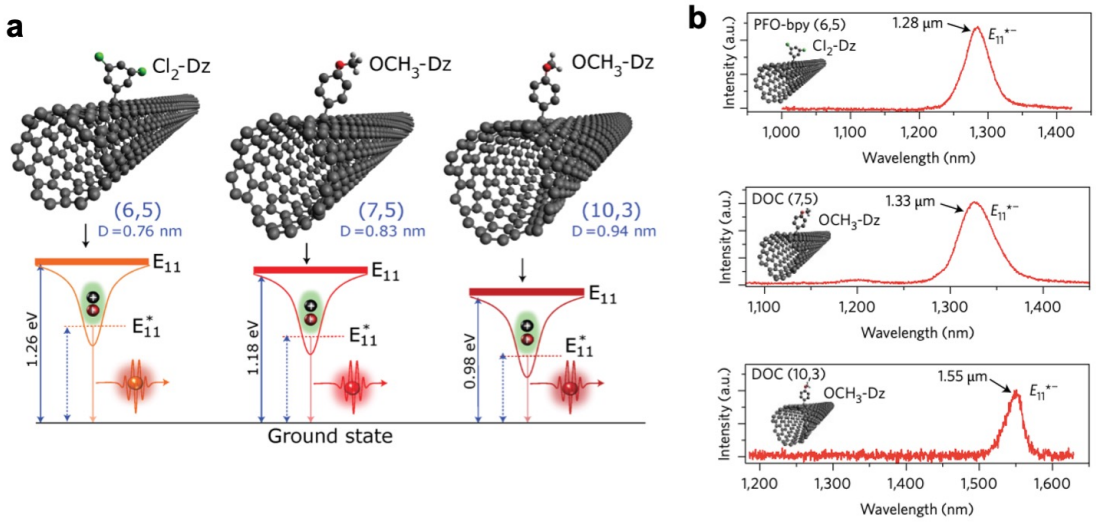

Figure 2.8 | Tunable defect-state emission in monochiral SWCNTs. a, Diagram of aryl-functionalized SWCNTs for tunable defect-state single-photon emission. The structure of a single covalently bound aryl-defect site for three different monochiral SWCNTs is shown. Corresponding band diagrams are illustrated below the structures, showing the tunable sp^3 defect trap states (E_{11}^*) that can trap and relax generated excitons for single-photon emission. **b,** Photoluminescence spectra of the different defect states illustrated in **a**. Reprinted by permission from Springer Nature: Nature Photonics,[159] Copyright (2017).

One of the shortcomings of the sp^3 defect system is the spectral broadening caused by the diversity of emitting states created through functionalization. However, aryl functionalization of 'zig-zag' SWCNTs causes defect states to become degenerate due to structural symmetry, resulting in single-photon emission bandwidth narrowing by a factor of three.[161] In order to consider the SWCNT sp^3 defect system suitable for practical SPE applications, important shortcomings must be addressed including PL intensity fluctuations, low quantum yields, and low photon indistinguishability. While efforts have been made to understand the origin of these issues,[162,163] practical solutions have yet to be demonstrated. In an alternative method of creating SWCNT-

based SPEs, micrometer-sized, air-suspended SWCNT have produced high-purity single photons at room temperature through diffusion-driven annihilation of mobile excitons. However, single photon purity varies with SWCNT chirality as well as suspended lengths, and simulations suggest the demonstrated SPE performance has significant room for improvement.[164]

2.2.2.3 Cavity-enhanced and plasmonically-enhanced SWCNT optical emitters

Monochiral SWCNT optical emitters are sensitive to local temperature, hot-carrier injection, and surface interactions, resulting in undesirable linewidth broadening and low quantum yields. However, their properties can be enhanced by increasing light-matter interactions through coupling with a microresonator structure (e.g., Fabry–Pérot microcavity or photonic crystal cavities). In weak emitter-resonator coupling, the radiative emission rate is enhanced by factors (i.e., Purcell factor) in excess of 10^2. The emission energy window of the coupled structure is given by the cavity modes (i.e., cavity feeding effect), resulting in narrow emission linewidths when compared with the free-space emission of SWCNT emitters.[11] Furthermore, cavity structures enable tuning of the emission wavelength by simply changing the cavity dimensions instead of changing the chirality of the SWCNT emitter. Although these SWCNT-microresonator structures are easily integrated with other components (e.g., waveguides) that are utilized in photonic circuit design,[165,166] their performance can suffer from sensitivity to processing and SWCNT-microresonator alignment. For further information on cavity structures integrated with SWCNT emitters, we refer the reader to the following article.[11] While high-speed, cavity-coupled emitters with narrow linewidths have been demonstrated using s-SWCNTs,[166] the use of monochiral species facilitates the study of SWCNT photophysics.

An example of unique photophysics in cavity-coupled monochiral SWCNT optical emitters is the realization of room-temperature exciton-polariton emission. This exciton-polariton emission was achieved through optically-pumped (6,5) SWCNTs embedded in a PFO-BPy copolymer matrix inside a planar metal-clad cavity. Large Rabi splitting was observed due to ultrastrong coupling, while polariton emission showed tunability across the entire telecom band.[167] In a later study, electrically-driven exciton-polariton emission at room temperature was realized by integrating a top-gate/bottom-contact transistor into a photonic microcavity. As shown in Figure 2.9, directional emission of these devices in the telecom range is controlled (1,060 – 1,530 nm) through cavity detuning. Most notably, the high level of optical emission suggests that reaching the polariton lasing threshold may be possible through further device optimization.[168] Similarly, another study used aligned (6,5) SWCNTs in a Fabry-Pérot microcavity to demonstrate that ultrastrong exciton-polariton coupling can be tuned through a simple rotation of the probe light polarization. This observation provides further insight into polariton anisotropic behavior and suggests that polariton emitters could be used in quantum information processing applications.[169]

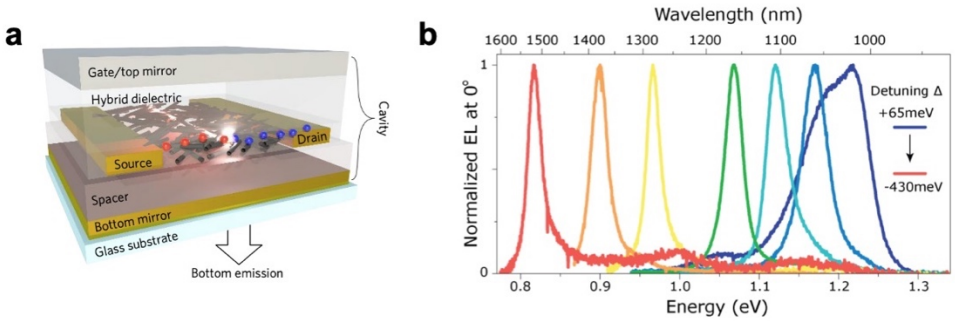

Figure 2.9 | Electrically-pumped SWCNT emitter. a, Schematic of microcavity-integrated light-emitting FETs using (6,5) SWCNTs. **b,** EL emission spectra at room temperature as a

function of cavity detuning. Reprinted by permission from Springer Nature: Nature Materials,[168] Copyright (2017).

Conventional phenomena, such as channel length scaling, have also been investigated. For example, an electrically-driven, light-emitting transistor using (8,3) and (8,4) SWCNTs has been integrated into a Fabry-Pérot cavity, where significant performance improvements were achieved through reduction of the channel length. Short channel length (0.5 μm) devices show strong emission at reduced biases, while cavity control enables narrow linewidth (~26 meV) and tuning of the emission in the telecom regime (1,180 – 1,443 nm).[165]

As an alternative emission enhancement approach, SWCNT coupling with plasmonic resonators has also been explored. In particular, periodic arrays of gold nanodisks coupled to (6,5) SWCNT films resulted in broad emission tunability (1,000 – 1,500 nm) and narrow linewidths (20 – 40 meV) through the Purcell effect. In addition, polarized and highly directional (divergence < 1.5°) emission was demonstrated despite the use of randomly distributed SWCNTs due to the dispersion properties of the plasmonic crystals.[40] In another study, plasmonic nanocavity arrays were coupled to (5,4) and (6,4) SWCNT excitons for large Purcell enhancements. Despite the small mode volumes, these optical emitters show Purcell factors up to 180, Purcell-enhanced quantum yield enhancement from 2% to 62%, ultra-narrow linewidths of 18 μeV, and 15 MHz photon emission rates.[170] These results demonstrate the potential of plasmonic resonators for monochiral SWCNT optical emitter enhancement and polarized light emission.

2.2.3 Photodetectors

In addition to electronic devices and optical emitters, on-chip photonic and optoelectronic systems require high-performance photodetectors. SWCNTs offer a number of distinct advantages in photodetectors including room-temperature operation, fast intrinsic response, wide bandgap tunability through chiral selection, polarization sensitivity along the nanotube axis, and compatibility with conventional fabrication.[12] Due to these intrinsic features, a large number of SWCNT-based photodetectors have been reported as delineated in recent comprehensive reviews.[5,12,171] Here, we focus on recent progress in SWCNT photodetectors that show promising results for integration into optoelectronic applications, such as barrier-free bipolar-diode (BFBD) photodetectors.

The BFBD photodetector design uses a SWCNT film with asymmetric Sc/Pd contacts to create a doping-free photodiode. The use of multiple virtual contacts (i.e., floating asymmetrical contact pairs in the channel) provides a parallel current path and modulates the channel potential, resulting in photovoltage signal multiplication with significantly improved signal-to-noise ratio. Additionally, BFBDs are capable of room-temperature operation, low power consumption, and high scalability due to the simplicity of their design.[171] For example, a BFBD photodetector using high-purity semiconducting SWCNTs has been demonstrated to operate at room temperature and zero bias. In this study, a total of 22,500 photodetectors were fabricated on a 2-inch Si substrate, achieving broadband response (785 – 2,100 nm), high detectivity (10^{11} Jones), and wafer-scale uniformity.[172] Furthermore, using a single (17,1) SWCNT, it was found that the conversion efficiency of the BFBD design is strongly dependent on the channel length, such that reducing the channel length down to 60 nm increases the conversion efficiency above 60%.[173] Additional performance improvements in the BFBD design have been demonstrated through the use of a thin

Y_2O_3 coating, which reduces forward/reverse current variance and increases photocurrent stability.[174] In related work, a single nanotube photodiode was integrated with a Fabry-Pérot cavity using asymmetrical Sc/Pd contacts. As shown in Figure 2.10, this design achieves a six-fold enhancement in optical absorption as well as higher suppression ratios. The integration of (8,4) and (8,3) SWCNTs into cavities further improves signal recognition and narrows the full width at half maximum (FWHM) of the target photoresponse.[175] Despite these advances, the sensitivity of SWCNT-based photodetectors has not reached the single photon limit as is needed in many quantum information technologies to complement SPEs.

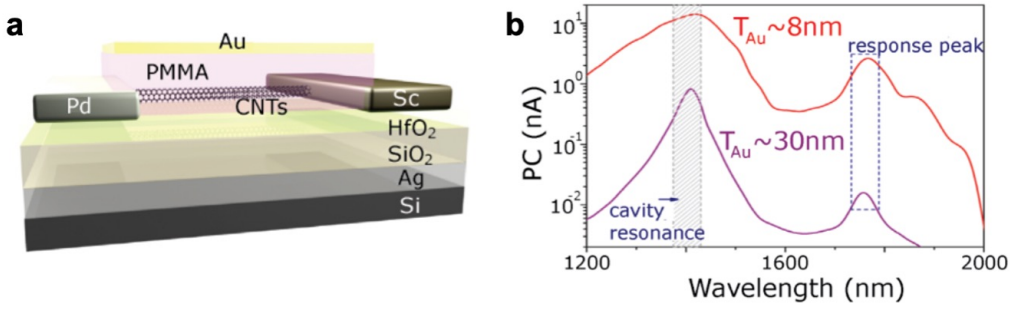

Figure 2.10 | Microcavity-integrated SWCNT photodetector. a, Diagram of a single-nanotube diode photodetector integrated in a metal-end-face Fabry-Pérot microcavity. **b,** Photoresponse of integrated devices with different Au mirror thicknesses, showing improvement in the suppression ratio at the SWCNT response peak. Reprinted with permission from [175]. Copyright 2016 American Chemical Society.

2.2.4 Optoelectronic integrated circuits

Modern communication technologies rely on photonic systems due to their ability to transmit information over long distances at high speeds and low losses. However, an emerging research area aims to create optoelectronic systems that replace traditional on-chip metal lines with photonic interconnects, using light to carry information and enhance data transfer rates over short

distances.[11,18] Due to the properties of SWCNTs, significant advances have been made in the fundamental building blocks of these emerging systems using both electronic-type and monochiral-enriched SWCNTs.[152,159,168,175] In this section, we consider recent progress towards the development of SWCNT-based optoelectronic ICs.

Integration of high-performance optical interconnects with SWCNT optical emitters and photodetectors is a prerequisite for these systems. In one demonstration, SWCNTs have been placed above photonic waveguides using dielectrophoresis, allowing near-field coupling of electrically-driven SWCNT emission. Although this work confirms that multiple emitters can be contacted in parallel to a single waveguide, the fabricated devices show high propagation loss (~12 $dB \cdot cm^{-1}$) and require high current levels to drive emission.[176] In another study using a similar waveguide-SWCNT integration scheme, few-chirality SWCNTs were found to have diameter-dependent photocurrent generation properties, such that large diameter SWCNTs only contribute to photocurrent generation when the waveguide is photoexcited.[177] Guided propagation and detection of telecom wavelengths signals have also been demonstrated.[177,178] However, other important factors for practical SWCNT-optical interconnects remain largely unexplored including reproducibility, tight modal confinement, and high-density integration of multiple input and output photonic channels.

Despite optical interconnect limitations, several SWCNT-based optoelectronic ICs have been fabricated. The first monolithic devices that performed logic functions with both electrical and optical inputs were realized using SWCNT-Si heterojunction photodiodes. Although high optoelectronic performance and crucial logic functions (e.g., AND gates and 4-bit digital-to-analog converters) were realized, the device relied on external optical stimulus for operation.[179]

Addressing this limitation, a follow-up study demonstrated the complete integration of an electrically-driven SWCNT-based optoelectronic IC operating at room temperature. In this case, CMOS-compatible fabrication methods were used to achieve vertical integration of the following three components: (1) electrically-driven optical emitters using chirality-enriched (8,3) and (8,4) SWCNTs; (2) photovoltaic detectors based on electronic-type-enriched SWCNTs; (3) SWCNT FETs. This 3D optoelectronic IC achieved parallel optical communication and fundamental computational functionality, such as the optoelectronic AND gate shown in Figure 2.11. While the vertical communication design can theoretically achieve high communication speeds on the order of $10 \cdot n^2$ Gbps for an n x n emitter/detector array, compatibility with other photonic elements (e.g., waveguides) was not addressed.[180]

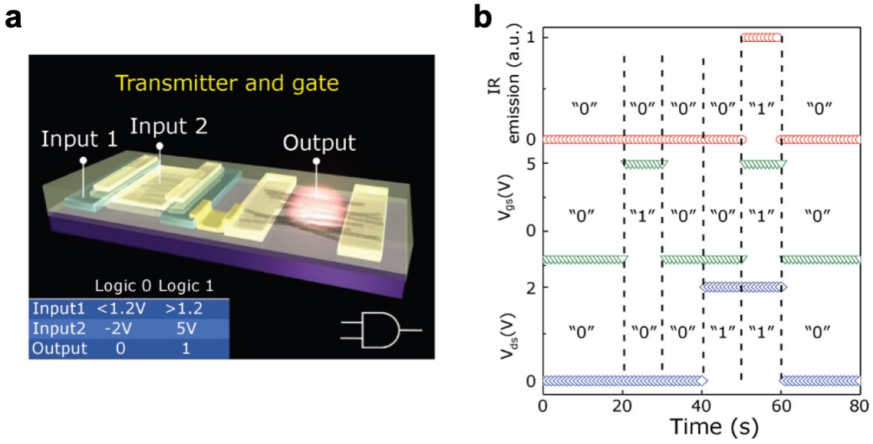

Figure 2.11 | Optoelectronic logic gate. a, Diagram of an AND optoelectronic gate composed of a SWCNT n-type FET, and an IR emitter using (8,4) and (8,3) SWCNTs. **b,** Input and output waveforms of the logic gate. This optoelectronic AND gate utilizes two voltages (V_{GS} and V_{DS}) as inputs and one optical output (IR emission). Reproduced from [180] licensed by CC BY 4.0.

SWCNT-based plasmonic interconnected circuits have also been achieved using electrically-driven surface plasmon-polariton sources and Au-strip plasmonic waveguides.[181]

Additional advances in this plasmonic interconnected circuit design enable 3D integration of plasmonic interconnects and electronic devices. This 3D optoelectronic IC design achieves several complex functional components including unidirectional receivers, wavelength-polarization multiplexers, and receivers integrated with signal-processing units.[182] Further development of the individual components of optoelectronic systems includes a polarization-sensitive telecom transceiver based on aligned SWCNTs,[183] and a highly-scaled photovoltaic receiver utilizing the BFBD design for efficient light amplification and attenuation.[184] Another key milestone was demonstrated through the integration of an electrically-driven SWCNT SPE with a photonic circuit. On-chip non-classical optical ($g^{(2)}(0) \sim 0.5$) emission, propagation, and detection were achieved at cryogenic temperatures using photonic waveguides and integrated superconducting nanowire single-photon detectors.[185] The use of scalable fabrication methods in this device establishes a route towards the development of nanoscale photonic systems for quantum information processing applications.

2.3 Progress in enantiomerically-pure SWCNTs

The wide variety of computing applications covered in Sections 2.1 and 2.2 are primarily enabled by advances in electronic-type and monochiral enrichment techniques. However, even single-chirality samples possess another structural degree of freedom since both right-handed and left-handed enantiomers are present. On the other hand, the realization of enantiomerically pure SWCNTs would enable additional applications based on their high sensitivity to circularly polarized light and chiral molecular species.[21,186] In this section, we discuss recent progress in SWCNT enantiomeric enrichment methods, characterization, and emerging applications.

Enantiomerically pure SWCNT samples have been particularly challenging to isolate since direct growth methods provide little to no enantiomeric enrichment. In contrast, solution-based post-processing purification methods have achieved enantiomeric separation, particularly when combined with chiral adsorbates.[10] Although enantiomeric separation has been achieved using molecular tweezers,[187] chiral polymers,[188] and countercurrent chromatography,[189] the most studied enantiomeric enrichment methods to date are DNA-assisted ATPE, non-linear DGU, and gel chromatography.

In DNA-assisted ATPE, enantiomeric separation has been achieved by exploiting the homochiral nature of ss-DNA for handedness selectivity.[190] DNA selectively interacts with specific SWCNT chiralities and enantiomers, forming DNA-SWCNT hybrids. These hybrids can then be separated into the hydrophobic or hydrophilic phase of either the PEG/polyacrylamide (PAM) or PEG/DX system. Through sequence control of the homochiral DNA, over 300 short ss-DNA sequences have been screened and 20 distinct SWCNT structures have been separated as shown in Figure 2.12. The resulting enantiomeric purity can be quantified as a function of chirality with circular dichroism (CD) spectroscopy, which showed that (6,5) SWCNTs achieved an enantiomeric excess of over 90%. However, relatively low separation yields limit the adaptation of this technique for large-scale chiral enrichment applications.

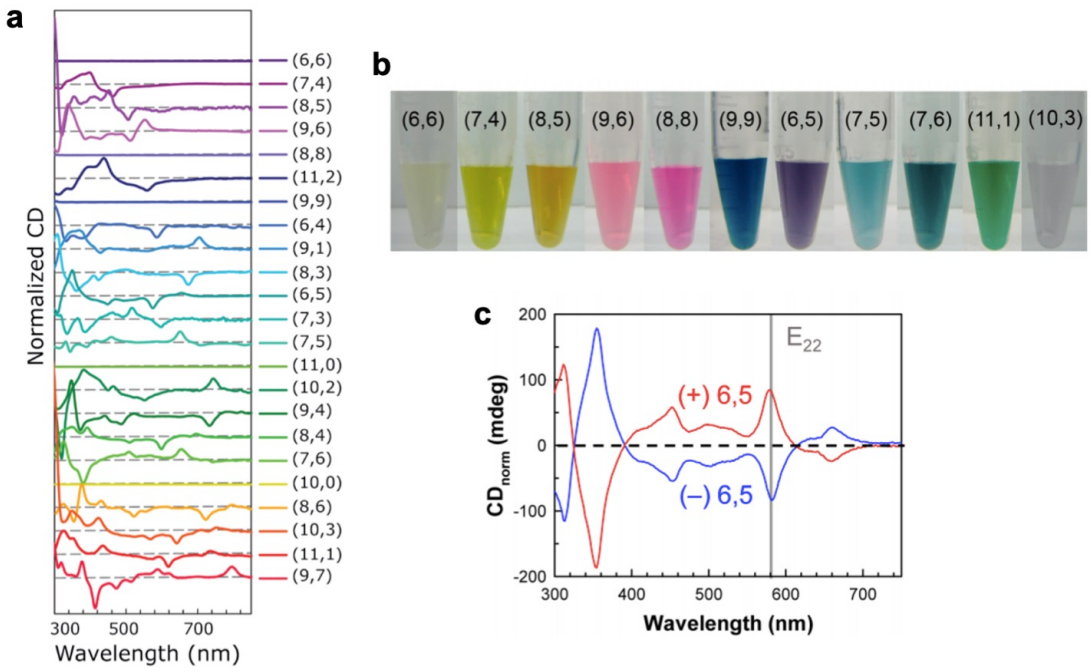

Figure 2.12 | SWCNT enantiomeric enrichment using ATPE. a, CD spectra of SWCNT species separated using ATPE with ss-DNA for handedness and helicity selectivity. **b,** Optical photograph of separated SWCNT species. **c,** CD spectra of separated (6,5) SWCNT enantiomers. Reprinted with permission from [190]. Copyright 2016 American Chemical Society.

To achieve enantiomeric separation with DGU, chiral surfactants are used to discriminate based on SWCNT handedness, creating small differences in buoyant density. The resulting SWCNT-surfactant mixture is then centrifuged within a density gradient medium, separating the SWCNT enantiomers based on their different isopycnic points. In the first DGU enantiomeric enrichment demonstration, the chiral surfactant sodium cholate and a linear density gradient were used to simultaneously separate SWCNTs by chirality and handedness in a single centrifugation step.[21] Similarly, enantiomeric separation for seven different monochiral species was achieved using a co-surfactant mixture (0.7% sodium cholate plus 0.175% sodium dodecyl sulfate) and a non-linear density gradient.[53] Notably, monochiral and enantiomeric separation was achieved in a

single non-linear DGU step despite starting with a SWCNT mixture with higher polydispersity (HiPco) than previous DGU publications (CoMoCAT). Figure 2.13 shows an optical photograph and vertical fluorescence spectra of the (6,5) SWCNT enantiomers that were isolated using the non-linear DGU method.

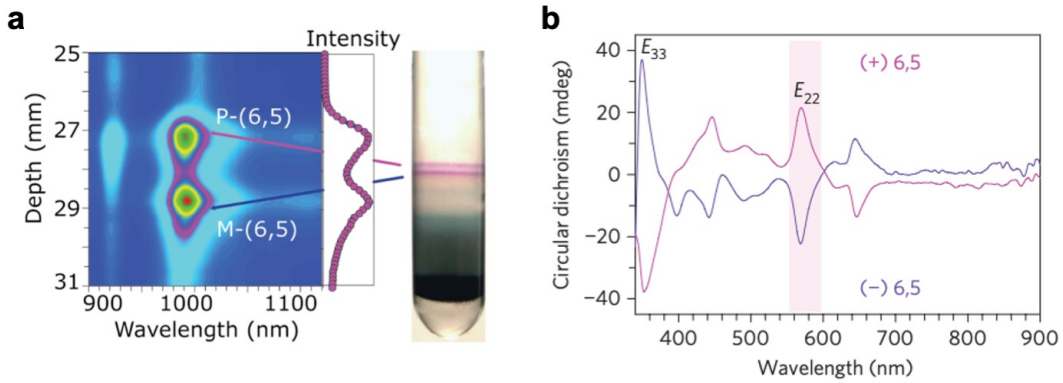

Figure 2.13 | SWCNT enantiomeric enrichment using DGU. a, Vertical fluorescence spectrum showing spatially separated (6,5) SWCNT enantiomer response at 783 nm excitation for sample separated using non-linear DGU. Also shown is an optical photograph of distinct (6,5) SWCNT enantiomer bands in a centrifuge tube following non-linear DGU. **b,** CD spectra of separated (6,5) SWCNT enantiomers. Reprinted by permission from Springer Nature: Nature Nanotechnology,[53] Copyright (2010).

In gel chromatography, enantiomeric enrichment is enabled by selective interaction of SWCNT enantiomers with chiral moieties in dextran-based gels (Sephacryl). In this case, mixed SWCNT species are dispersed with sodium cholate and sodium dodecyl sulfate, which are then passed through a multicolumn gel chromatography system to achieve the separation of nine semiconducting monochiral enantiomer species.[191] This method has been further extended to enantiomeric separation of metallic species through m-SWCNT pre-selection, surfactant reduction, and longer gel columns.[192] Enantiomeric enrichment can be additionally enhanced

through the use of stepwise elution and the addition of an additional surfactant (i.e., sodium deoxycholate), which leads to the simultaneous separation of 12 different SWCNT enantiomers with purities over 90% for most of the separated species.[193] Further optimization of this triple-surfactant system also allows monochiral enantiomer separation in a single step,[194] as well as large-scale enantiomeric separation.[186] Figure 2.14 shows a schematic of the large-scale, triple-surfactant gel chromatography system, as well as CD characterization of separated (6,5) SWCNT enantiomers. To date, GC has achieved monochiral enantiomeric enrichment with simultaneous milligram-scale throughput, high yield (up to 28%), and relatively high enantiomeric purity (79-84%),[186] making GC the most optimized enantiomeric enrichment technology to date.

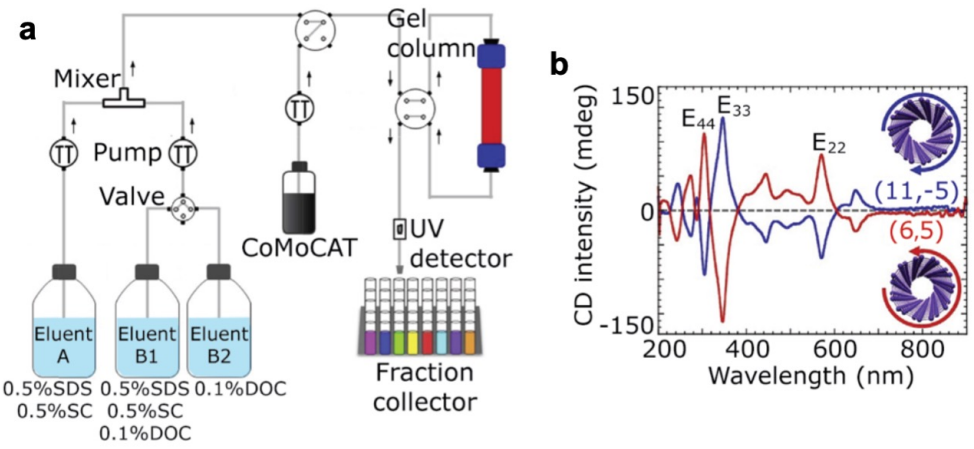

Figure 2.14 | SWCNT enantiomeric enrichment using gel chromatography. a, Schematic of triple surfactant stepwise elution dextran-based gel chromatography. The liquid delivery direction is indicated by arrows. **b,** CD spectra for separated (6,5) SWCNT enantiomers. Reprinted from [186], Copyright (2018), with permission from Elsevier.

These relatively high enantiomeric purity levels have enabled several fundamental breakthroughs in SWCNT optical property characterization. In particular, characterization of

SWCNT solutions with high enantiomeric purity result in optical absorption and CD spectra with strong intensities. As a result, numerous optical transitions become apparent that are not commonly observed, allowing for experimental confirmation of theoretically predicted diameter scaling behavior of E_{ii} and E_{ij} transitions.[193] In another study, enantiomerically-enriched (6,5) SWCNT solutions were combined with an enantiomer-sensitive dispersant, flavin mononucleotide (FMN). Using optical absorbance and CD spectra, FMN was observed to induce a handedness-dependent shift in the E_{11} optical transition that is linearly correlated with enantiomeric purity.[195] Figure 2.15 shows an example CD spectra and how its intensity changes for different (6,5) SWCNT enantiomer concentrations when coupled to FMN. This strategy enables direct measurement of enantiomeric purity for any mixture of (6,5) SWCNT enantiomers using only CD characterization, suggesting a generalized method for high-throughput SWCNT enantiomeric purity characterization.

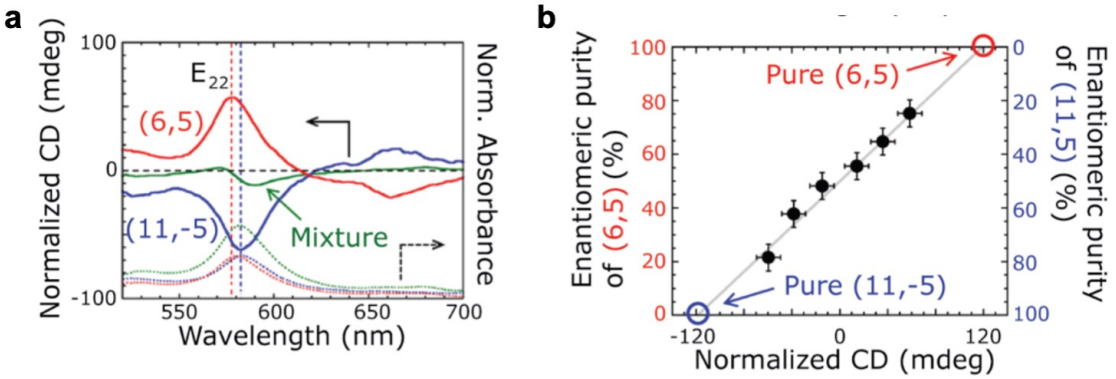

Figure 2.15 | SWCNT enantiomeric purity characterization using FNM. a, Normalized CD and optical absorption spectra of individual (6,5) SWCNT enantiomers and their mixture in FNM solution. A considerable difference in the CD and absorption peaks is observed. The absorption mixture peak can be fitted to obtain the individual enantiomer peaks as shown in the inset for the E_{11} peak. **b,** Enantiomeric purity estimates as a function of mixture CD peak intensities. Reprinted with permission from [195]. Copyright 2017 American Chemical Society.

While SWCNT enantiomeric enrichment and characterization have been widely studied, the number of applications that exploit enantiomerically pure SWCNTs remains limited. An exception is the use of (6,5) SWCNT enantiomers to create a chiral space in a glassy carbon electrode (GCE). Using differential pulse voltammetry (DPV), this electrode shows an enantioselective response for 3,4-dihydroxyphenylalanine (DOPA) enantiomers (L-DOPA and D-DOPA), which is sufficient to both distinguish each enantiomeric species and determine DOPA enantiomeric excess.[14] Figure 2.16 shows a schematic of this DOPA enantiomeric sensing strategy, as well as DPV spectra of P-(6,5) SWCNT/GCE with different mixtures of L-DOPA/D-DOPA concentrations. This sensor suggests the potential of SWCNT enantiomers for highly selective biological sensing, which is expected to inspire further investigations into SWCNT enantiomer applications.

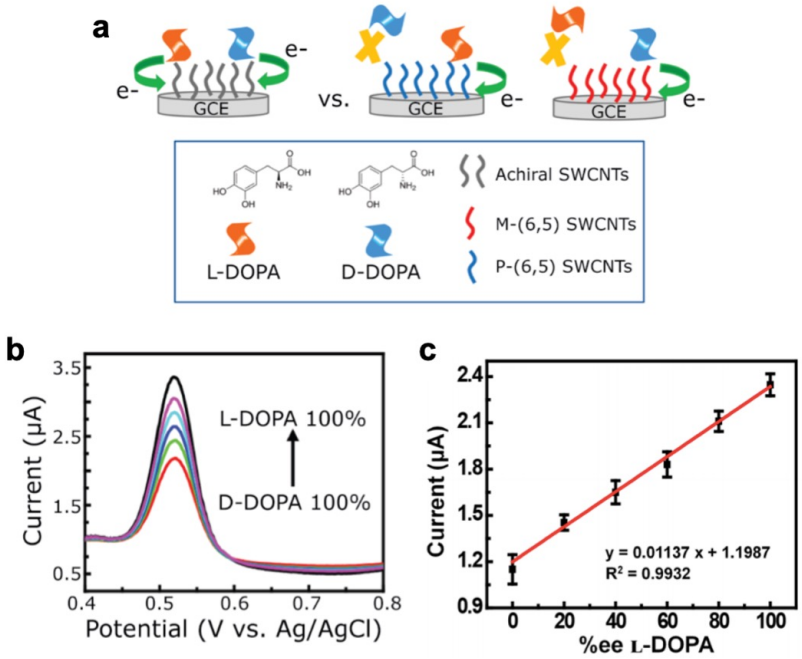

Figure 2.16 | Electrochemical enantiomer recognition sensor. a, Schematic of the electrochemical sensor using monochiral SWCNT enantiomers to create a chiral space on a GCE for enantiomer recognition. **b,** DPV spectra of P-(6,5)-SWCNT/GCE for DOPA racemic mixture

solutions with varying L-DOPA%. **c,** Plot of DPV peak current as a function of L-DOPA concentration in solution. Reprinted with permission from [14]. Copyright 2019 American Chemical Society.

Chapter 3: Carbon nanotube true random number generator

With the growing adoption of interconnected electronic devices in consumer and industrial applications, there is increasing demand for robust security protocols when transmitting and receiving sensitive data. Towards this end, hardware true random number generators (TRNGs), commonly used to create encryption keys, offer significant advantages over software pseudo-random number generators. However, the vast network of devices and sensors envisioned for the Internet of Things will require small, low-cost, and mechanically flexible TRNGs with low computational complexity. These rigorous constraints position solution-processed semiconducting single-walled carbon nanotubes (SWCNTs) as leading candidates for next-generation security devices. Here, we demonstrate the first TRNG using static random access memory (SRAM) cells based on solution-processed SWCNTs that digitize thermal noise to generate random bits. This bit generation strategy can be readily implemented in hardware with minimal transistor and computational overhead, resulting in an output stream that passes standardized statistical tests for randomness. By using solution-processed semiconducting SWCNTs in a low-power, complementary architecture to achieve TRNG, we demonstrate a promising approach for improving the security of printable and flexible electronics.

3.1 Random number generators in security applications

The proliferation of networked physical devices, such as wearable technologies and embedded electronic systems, has enabled unprecedented levels of data collection, exchange, and analysis.[196,197] As more interconnected devices are developed to manage personal and sensitive information, there is a growing need for robust security primitives. Random number generators are of paramount importance in these security applications since they are commonly combined with

other primitives to generate encryption keys.[198-200] While software-based pseudo-random number generators are often employed for this purpose, they are inherently non-random in nature with outputs that can be reproduced if the initial seed is known. In contrast, hardware-based true random number generators (TRNGs) use natural phenomena (e.g., thermal noise) to produce outputs that can be truly random, thus enabling superior encryption. The emerging Internet of Things would thus greatly benefit from the enhanced security of integrated TRNGs.[47,196,197]

Portable networked devices further require small-scale and low-cost security hardware components. In addition, emerging wearable technologies often demand low-power computing elements that are ultra-thin and mechanically flexible.[201,202] As a result, existing hardware-based TRNG implementations based on conventional rigid semiconductor substrates and processing methods have found limited utility in flexible electronics applications. For example, optical TRNGs require integrated lasers, photon detectors, and substantial computational overhead to generate random bit streams.[203-205] Similarly, small-scale TRNGs based on crystalline semiconductors are not inherently flexible and require expensive processing.[206,207] In contrast, semiconducting single-walled carbon nanotubes (SWCNTs) are promising candidates for next-generation security devices due to their solution-processability, chemical stability, and superlative electronic properties.[208-210] With these attributes, semiconducting SWCNTs have been successfully employed in a series of high-performance,[211,212] printed,[213,214] and/or flexible electronic applications.[211,215] To date, SWCNT-based security device demonstrations have been limited to physically unclonable functions (PUFs) that create static, chip-unique cryptographic keys.[216] However, in contrast to TRNGs, the demonstrated PUFs are unable to perform critical

tasks commonly used in encryption protocols, such as dynamically generating secure keys, cryptographic nonces, and random padding bits.

Here, we demonstrate the first TRNG based on a solution-processed semiconductor by employing low-power, complementary SWCNT static random access memory (SRAM) cells.[217] This approach requires minimal computational overhead to produce highly random bit streams as confirmed through a series of rigorous tests including the National Institute of Standards and Technology (NIST) randomness statistical test suite (STS)[218] and the TestU01 battery tests.[219] This work thus presents a promising methodology for improving security in the rapidly growing global network of interconnected electronic and sensing devices.

3.2 Processing optimization for the fabrication of SWCNT SRAM cells

Previous SWCNT thin-film transistor (TFT) efforts have resulted in the realization of complex complementary circuits, such as SRAM cells, with reliable operation and performance.[217,220] Building from that precedent, Figure 3.1 shows an optical micrograph of a SWCNT TFT-based complementary SRAM cell and its corresponding circuit-level diagram. The SRAM cell is composed of two p-type (highlighted orange) and two n-type (highlighted green) TFTs that correspond to two cross-coupled inverters with output (Q and $\overline{Q}$) and supply (V_{DD} and GND) terminals. Two access p-type TFTs (highlighted blue) are controlled through the wordline (WL) terminal and tie the bitline (BL and $\overline{BL}$) terminals with the inverter output terminals. A TFT channel length of 20 μm and a 2:1 width ratio (300 μm:150 μm) between the p-type pull-up and n-type pull-down TFTs are used to achieve optimal performance.

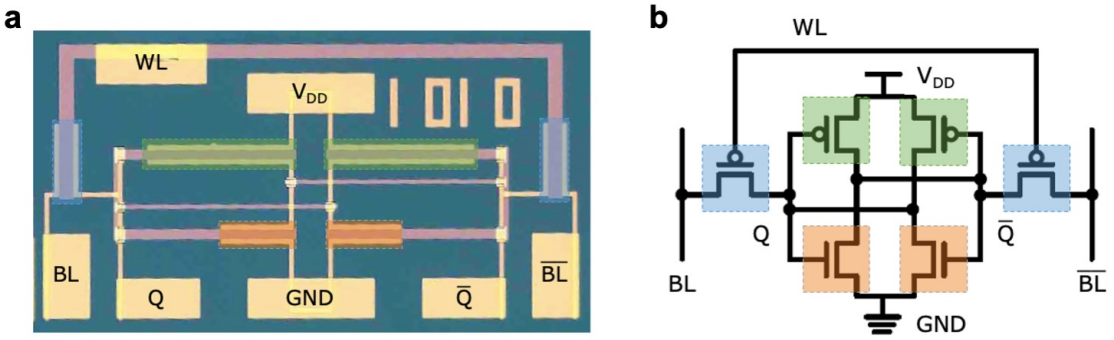

Figure 3.1 | SWNT complementary SRAM cell. a, Optical micrograph of a fabricated SWCNT complementary SRAM cell, showing labeled contact terminals, p-type inverter pull-up TFTs (orange), n-type inverter pull-down TFTs (green), and bitline access TFTs (blue). **b**, Corresponding circuit-level diagram of the SRAM cell shown in part (**a**). Reprinted with permission from[75]. Copyright 2019 American Chemical Society.

The SRAM cell arrays were fabricated using previously reported methods.[220-222] As can be seen in the cross-sectional schematic of a SWCNT TFT shown in Figure 3.2a, the fabricated devices employ a local backgate geometry with sorted, semiconducting SWCNTs (99% purity) as the semiconducting channel. As shown by atomic force microscopy in Figure 3.2b, the SWCNT channel exhibits a random network morphology with a linear density of approximately 10 SWCNTs/μm. After doping the semiconducting channel, a 50 nm Al_2O_3 encapsulation layer is deposited to ensure dopant stability and thus long device lifetime under ambient conditions. All of the fabrication steps can be performed on polymer substrates,[223-225] enabling SRAM fabrication for mechanically flexible applications. Additional fabrication details are summarized below.

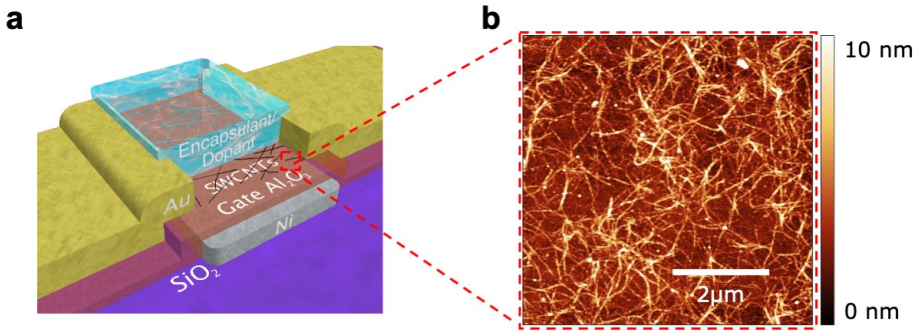

Figure 3.2 | SWNT TFT in SRAM cell. a, Cross-sectional diagram of a SWCNT TFT fabricated using a semiconducting SWCNT channel, p-type or n-type dopant layer, and Al_2O_3 encapsulation layer. **b,** Atomic force microscopy image of the SWCNT channel showing a random network morphology. Reprinted with permission from[75]. Copyright 2019 American Chemical Society

Device fabrication was performed on a p-type boron-doped Si(100) substrate with 300 nm SiO_2 layer. Local backgates were defined using photolithography and thermal evaporation of Ni (25 nm). A 10 nm Al_2O_3 gate oxide layer was deposited using trimethylaluminum (TMAl) and water precursors at 150°C with a Cambridge NanoTech atomic layer deposition (ALD) system. Photolithography and reactive ion etching (40 sccm Ar and 10 sccm CF_4 environment, 100 W for 6 min) define gate contact vias through the gate oxide layer. Residual surface oxide from the Ni backgate was removed under Ar plasma in an AJA Orion sputtering chamber, followed by sputtering Ag (30 nm) to create a via contact. Photolithography and thermal evaporation of Cr/Au (1 nm/50 nm) defined drain and source contacts. Sorted semiconducting SWCNTs with 99% purity were transferred to the substrate using a previously published procedure.[217] Lithography and reactive ion etching (20 sccm O_2, 100 W for 15 s) were used to define the semiconducting SWCNT channels. Samples were then transferred to an inert environment (N_2 glovebox) and vacuum annealed at 230°C for 1h. Shipley S1813 photoresist was deposited (spincoat, 3000 rpm. for 60 s) and baked (110°C for 60 s) before removing the

sample from the inert environment. The sample was subsequently moved to ambient conditions into a cleanroom, where the S1813 was patterned to define p-type channels using standard photolithography techniques. The sample was again moved into an inert environment and vacuum annealed under the same conditions. The benzyl viologen n-type dopant was prepared using a previously published procedure.[217,221,222] About 100 nm of this n-type dopant was deposited (spincoat, 1000 rpm for 60 s) and baked (90°C for 1 min) before removing the sample from the inert environment. A 50 nm Al_2O_3 encapsulation layer was finally deposited using TMAl and water precursors at 110°C with a Cambridge NanoTech ALD system.

3.3 Bit generation through tunable doping, encapsulation and biasing

In a typical SRAM cell, a single bit is stored within the cross-coupled inverters while power is supplied. When the wordline access transistors are turned on, the bitlines are used to perform read or write operations on the stored bit. However, when power is initially supplied to an SRAM cell, its binary memory state is unknown because symmetry of its cross-coupled inverters leads to a metastable state. This metastability is resolved when thermal noise fluctuations in the transistors drive the system into a stable “0” or “1” voltage level, leading to digitization of the thermal fluctuations. We leverage this digitization of inherently random physical noise to generate a sequence of truly random bits. Figure 3.3 summarizes how SRAM cells are operated as TRNGs using this principle.

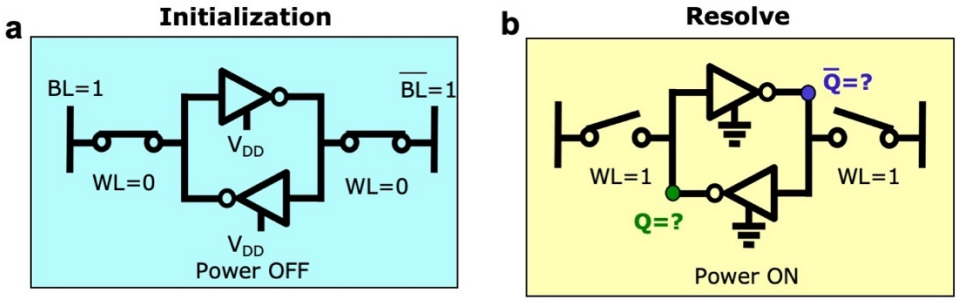

Figure 3.3 | SRAM operation as a bit generator. Gate-level diagram showing SRAM cell biases during the (**a**) initialization and (**b**) resolve steps of bit generation. When the wordline access transistors are turned off and the power to the cross-coupled inverters is turned on, the inverter outputs (Q and $\overline{Q}$) resolve to a complementary binary state dependent on thermal noise fluctuations. The third terminal in each inverter represents the GND supply terminal. Reprinted with permission from[75]. Copyright 2019 American Chemical Society

During the initialization step, wordline access p-type transistors are turned on (WL = 0 V), both bitlines are biased to V_{DD} (BL = $\overline{BL}$= 1.5 V), and the cross-coupled inverters are powered off (GND = V_{DD} = 1.5 V). In the resolve step of an initialized cell, power is supplied to its cross-coupled inverters (GND = 0 V) while wordline access transistors are turned off (WL = V_{DD} = 1.5 V), causing the output of each inverter (Q and $\overline{Q}$) to be randomly driven toward a stable complementary binary state by thermal noise fluctuations. A sample output of the resulting SRAM cell bit generation is shown in Figure 3.4. As expected, Q and $\overline{Q}$ are both in a high state during the initialization step, but exhibit complementary behavior during the resolve step. The measured voltage output of Q during each resolve step is then translated into a binary bit (i.e., high voltage = '1'; low voltage = '0'). Because the WL and GND voltage inputs act like complementary clock signals, this approach allows multiple SRAM cells to be operated synchronously,[226] enabling scalable bit generation throughput. Further testing details are provided below.

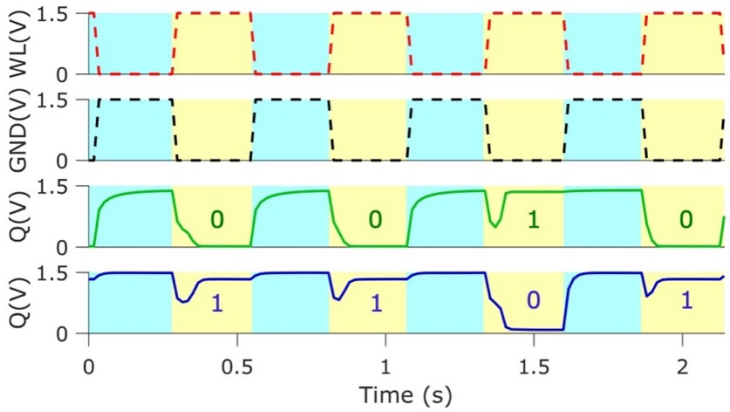

Figure 3.4 | SRAM bit generator output. Sample input (WL) and output (Q and $\overline{Q}$) voltages for multiple initialization/resolve steps. The stable analog output voltage level during each resolve step is interpreted into a single bit, resulting in complementary bit sequences for Q and $\overline{Q}$. Reprinted with permission from[75]. Copyright 2019 American Chemical Society

Bits generated by the SWCNT SRAM cells were collected under ambient conditions using a Keithley 4200-SCS parameter analyzer, two Keithley 2400 source measurement units (SMU), and a Cascade Microtech Summit 1200 semi-automatic probe station. The setup was used to: (1) apply constant V_{DD} and bitline voltages; (2) sweep wordline and ground voltages; (3) measure the output voltages at each inverter. A custom MATLAB script was used to analyze and convert the collected inverter output into binary sequences.

3.4 Tuning of output bit streams

Figure 3.5 shows a representative sample (136 initialization and resolve steps) of WL and Q voltages for a simulated and measured SRAM cell operating as a TRNG with a skew towards a logical high state of Q. In particular, a voltage offset between BL and $\overline{BL}$ is chosen such that Q resolves to a logical high state for ~95% of the generated bits. On the other hand, Figure 3.6 shows simulated and measured outputs for the same SRAM cell with a BL-$\overline{BL}$ voltage offset such that it

operates with no skew (i.e., a fair and balanced distribution). These results exhibit good agreement between simulation and experiment, confirming the validity of the circuit modeling. Further details regarding how annealing affects TRNG performance and how to control TRNG skew can be below and prior literature.[220]

In addition to thermal noise fluctuations, fabrication inhomogeneity results in variability of the on-state currents in an SRAM cell between its six transistors. Therefore, an SRAM cell operating as a TRNG with equal voltages on both BL and $\overline{\text{BL}}$ is likely to result in an output bias towards a particular logical state on Q. While this skew can be advantageous in some applications,[226] it can be tuned by applying a voltage offset between the BL and $\overline{\text{BL}}$ voltages during bit generation. Given that the output bias is proportional and sensitive to the processing variability, the BL-$\overline{\text{BL}}$ voltage offset required to tune the output varies from cell to cell. Both our experimental and simulated results require, on average, a BL-$\overline{\text{BL}}$ voltage offset in the range of ±100 mV to cause the change in skew shown between Figure 3a and Figure 3b. However, the resulting output bias towards a particular logical state is effectively random, such that predictions of the individual BL-$\overline{\text{BL}}$ voltage offsets from cell to cell are impractical. To improve upon this variability and enable higher levels of integration in future designs, the entropy of the digital output from the TRNG can be actively monitored and controlled through adjustments to the BL-$\overline{\text{BL}}$ voltage offset. Such active feedback designs are commonly implemented in more complex and commercially available TRNGs.[227-229]

The output signal of the SRAM-based TRNG is enabled by stable n-type doping and encapsulation.[217] Systematic studies of the viologen-SWCNT system have been previously reported,[221,222] and best practices for the vacuum annealing procedures have been followed. For

small changes in temperature, this performance variation can be compensated by adjusting the BL-$\overline{\text{BL}}$ voltage offset, but large changes in temperature will result in doping inappropriate for SRAM operation. For applications that require operation at elevated temperatures, previously demonstrated tunable n-type doping[221] would enable operation for specific temperature ranges.

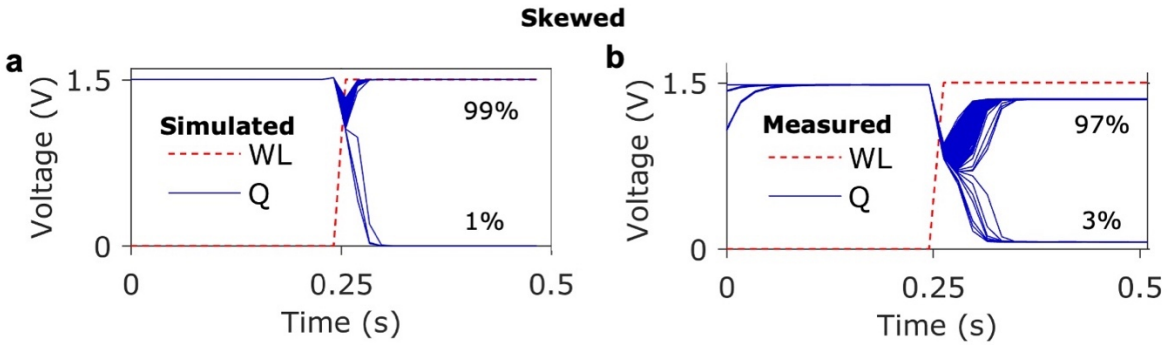

Figure 3.5 | Skewed output from SRAM bit generation. (**a**) Simulated and (**b**) measured output from an SRAM cell functioning as a TRNG where the BL-$\overline{\text{BL}}$ voltage offset creates a skew towards a logical high state for Q. Reprinted with permission from[75]. Copyright 2019 American Chemical Society

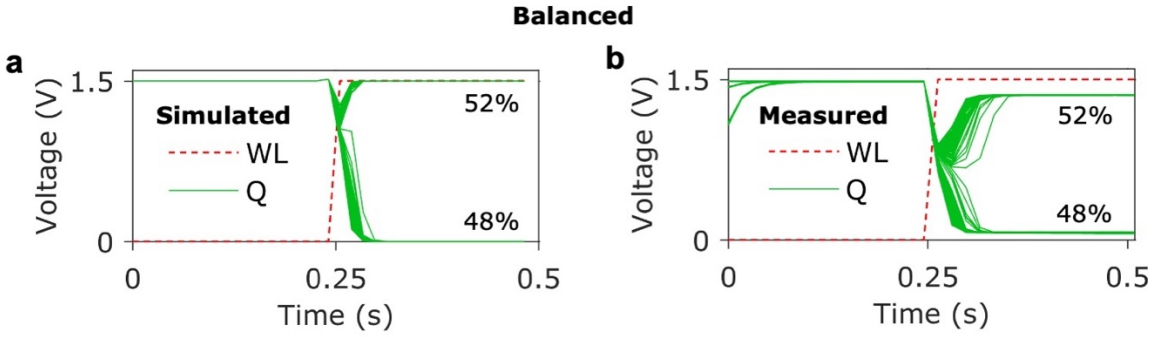

Figure 3.6 | Balanced output from SRAM bit generation. (**a**) Simulated and (**b**) measured output from an SRAM cell but with a BL-$\overline{\text{BL}}$ voltage offset such that it operates with minimal skew. Reprinted with permission from[75]. Copyright 2019 American Chemical Society

Using this experimental procedure, a total of 61,376 bits were collected from multiple SRAM cells. For this bit stream, the BL-$\overline{BL}$ voltage offsets were chosen for each SRAM cell to maximize the randomness of the post-processed output using the well-established von Neumann algorithm.[230] The von Neumann algorithm was chosen since it can be easily implemented in hardware and is widely used in traditional TRNGs. Importantly, the SWCNT SRAM cell requires no additional post-processing or active feedback to be implemented as a 3. Further details on bit collection are shown in Table 3.1 below.

Table 3.1 | Bits collected from SWCNT SRAM devices following post-processing

SRAM Cell ID	Bits Collected
0606	1,955
0613	2,860
0707	18,298
0807	4,418
1010	14,504
1515	12,151
2121	7,225
Total[a]	61,411

[a]The outputs are combined, but due to input constraints only the first 61,376 bits and 61,408 bits are used with the NIST statistical test suite and TestU01 software, respectively, for statistical testing of randomness. Reprinted with permission from[75]. Copyright 2019 American Chemical Society.

To visualize the effectiveness of this random bit generation and post-processing scheme, Figure 3.7 shows 75 × 75 bitmaps for sample raw (left) and post-processed (right) bit sequences. The bitmaps are created by populating two 75 × 75 matrices in reading order (left-to-right, top-to-bottom) with their corresponding bit sequences, where each element in the array corresponds to a pixel, and the value of the pixel indicates its color (‘0’ corresponds to white, ‘1’ corresponds to

blue or green). While the bitmap for the raw data is skewed and contains long streaks, no identifiable patterns can be distinguished in the post-processed data bitmap, qualitatively suggesting a high degree of randomness.

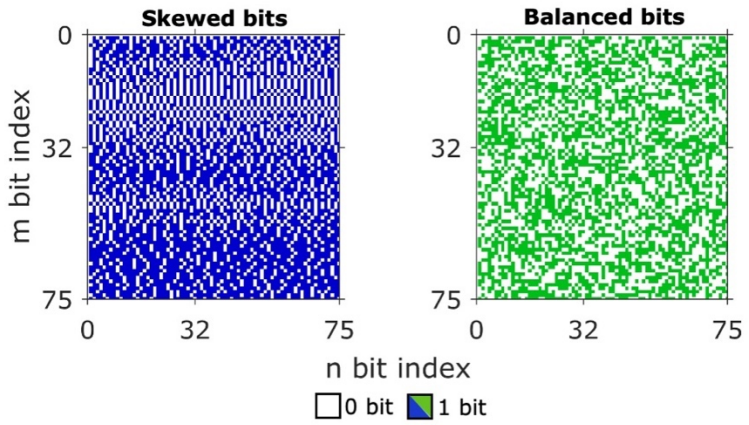

Figure 3.7 | Bitmaps of output from SRAM bit streams. Bitmaps for sample raw, skewed (blue) and post-processed, balanced (green) bit streams are created by populating two 75 × 75 matrices in reading order (left-to-right, top-to-bottom) with their corresponding bit sequences. A white or colored bit corresponds to a '0' or '1' bit, respectively. Reprinted with permission from[75]. Copyright 2019 American Chemical Society.

For a more quantitative assessment of randomness, a histogram of binned data can be compared with the expected theoretical distribution for a random bit sequence. All of the post-processed bits ("Balanced") and a representative sample of raw bits of equal length ("Skewed") are divided into 20-bit segments. The segments are then binned according to the average bit values of their constituent bits. The histograms in Figure 3.8 represent the frequency of bit values for each corresponding data set. Because a truly random bit sequence is equivalent to the sequence of independent Bernoulli trials for a fair coin, we compare our results with an appropriately scaled binomial probability density function ("Binomial"). The post-processed bit sequence closely

matches the expected binomial distribution, again suggesting a high degree of randomness, whereas the raw bit sequence shows a higher mean and lower standard deviation than expected.

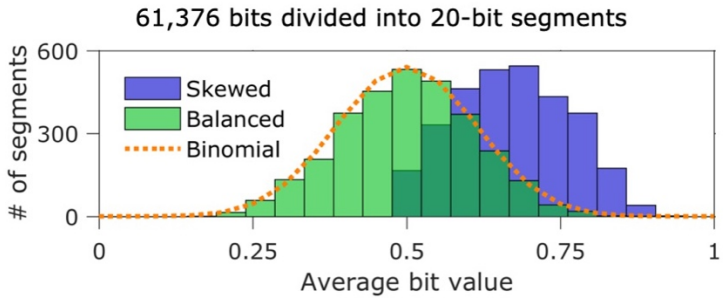

Figure 3.8 | Average bit values of 20-bit segments from bit generation. Histograms of average bit values when the raw ("Skewed") and balanced ("Balanced") bit streams are divided into 20-bit segments. The expected binomial probability distribution function is also shown for comparison. Reprinted with permission from[75]. Copyright 2019 American Chemical Society.

3.5 Randomness testing

To further quantify the level of randomness, the post-processed bit stream was subjected to the National Institute of Standards and Technology (NIST) randomness statistical test suite (STS).[218] For statistically significant results, the post-processed bit stream was divided into 56 sequences (i.e., the tests were performed 56 times on individual 1096-bit long sequences). Figures 3.9-12 show the results from four of the NIST STS randomness tests on (left, panels a) the post-processed bit streams and (right, panels b) sample raw data. In the frequency test, bits are assigned a value of +1 or -1, and cumulative sums are calculated for each sequence. Figure 3.9 illustrates the frequency test, where individual plot lines correspond to the running sums of the sequences tested. Evidently, the plot lines are clustered within the expected region for a random sequence.

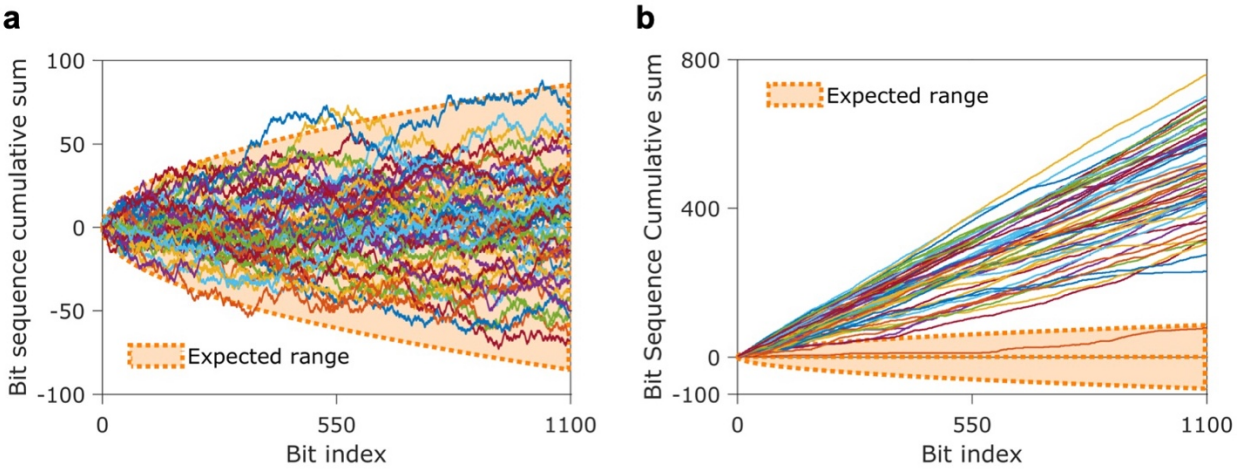

Figure 3.9 | NIST STS frequency test. Illustration of the frequency test on (**a**) balanced bits and (**b**) a representative sample of raw bits divided into 56 1096-bit long sequences. Each plot line represents the running sum for each of the 56 bit sequences tested, where bits are assigned values of -1 or +1. The highlighted range represents the expected sum value for a random bit sequence. Reprinted with permission from[75]. Copyright 2019 American Chemical Society.

We further tested for randomness with the longest run of ones in a block test, which partitions the bit sequence into M-bit blocks, determines the length of the longest consecutive run of "1" bits in each block ("Balanced"), and compares the resulting run occurrences with what would be expected from a random sequence ("Expected"). Figure 3.10 shows the results of this test using a block size of M = 8 bits. The bar height and superimposed error bars represent the average and standard deviation of the results, respectively, for the 56 sequences tested. The experimental results again show clear agreement with the expectations for a random sequence.

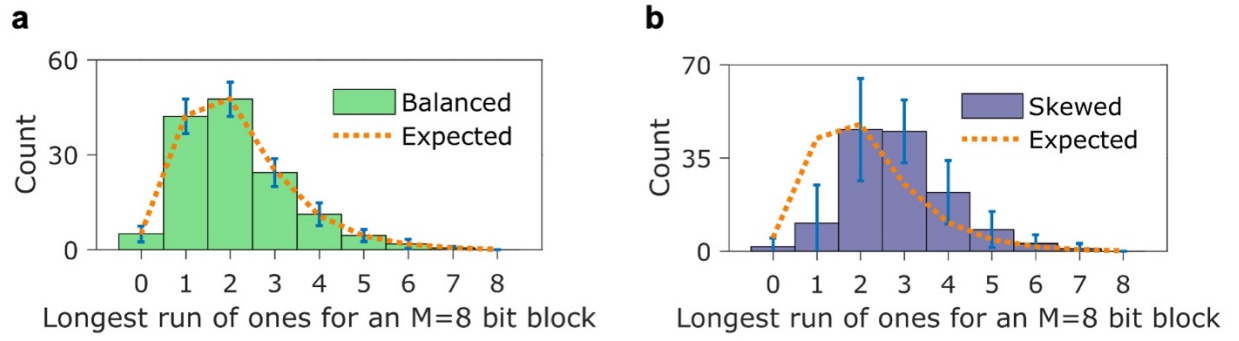

Figure 3.10 | NIST STS longest run of ones test. Illustration of the longest run of ones test, where the lengths of the longest consecutive runs of "1" bits of M-bit blocks in the sequences are counted. The resulting run occurrences from (**a**) balanced bits ("Balanced") and (**b**) sample raw bits ("Skewed") are compared with what would be expected from a random sequence ("Expected") The bar height and error bars represent the average and standard deviation from the results of the 56 bit sequences tested. Reprinted with permission from[75]. Copyright 2019 American Chemical Society.

A balanced sequence can still fail to be random if the output is skewed towards specific m-bit patterns. Thus, the serial test counts the frequency of all possible overlapping 2^m m-bit patterns in a sequence. Figure 3.11 illustrates the results of the serial test using m = 4 bits. The expected results for a random sequence, which has a uniform distribution, are also plotted in Figure 3.11 and confirm that the experimental bit stream passes the serial test of randomness.

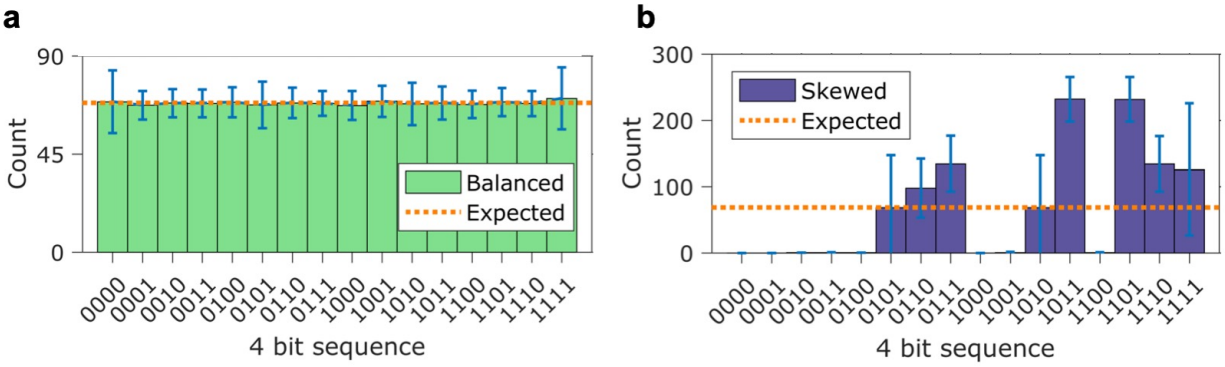

Figure 3.11 | NIST STS serial test. Illustration of the serial test, which calculates the frequency of m-bit patterns in a sequence. The results from (**a**) balanced bits ("Balanced") and (**b**) sample

raw bits ("Skewed") are compared with what would be expected from a random sequence ("Expected"). Reprinted with permission from[75]. Copyright 2019 American Chemical Society.

To expose possible periodic features, the spectral output of the discrete fast Fourier transform (FFT) test is shown in Figure 3.12. The FFT test calculates the percentage of sequence peak values below the 95% peak value threshold expected for a random sequence. Periodic components are likely to be present if the calculated percentage significantly deviates from 95%. Each plot line corresponds to a sequence, and the percentages on the right of the figure indicate the proportion of peaks below or above threshold. The experimental value of 94.99% agrees well with the 95% expectation for a truly random sequence. Further details on the NIST tests are provided below.

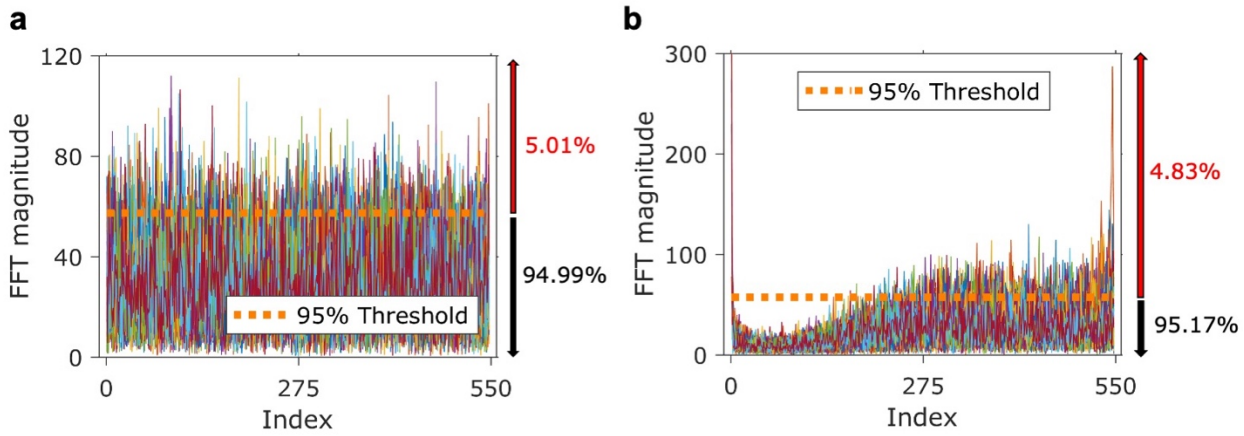

Figure 3.12 | NIST STS FFT test. Illustration of the fast Fourier transform (FFT) test, showing the resulting spectra for all 56 bit sequences tested. Percentage values on the right indicate the proportion of peaks values below and above the 95% threshold for all (**a**) balanced bits and (**b**) sample raw bits tested. A random bit sequence is expected to have 95% of its peaks below the indicated threshold (dashed orange line). Reprinted with permission from[75]. Copyright 2019 American Chemical Society.

The NIST statistical test suite software recommends testing a minimum of 55 bit sequences in order to obtain statistically significant results. Following this recommendation and minimum

bit requirements for the different tests, the collected bits following von Neumann post-processing are divided into 56 bit sequences with each sequence consisting of 1096 bits.

The frequency test is the first of these tests, and must be passed in order to pass any subsequent test. In the frequency test, '0' and '1' bits are assigned a value of +1 and -1, respectively. The assigned values for each sequence are added sequentially, and their cumulative sums are used to compute p-values for this test. Because the frequency test on a random bit sequence emulates a one-dimensional random walk, its final sum should not significantly deviate from zero and is expected to be within a predictable range of values. Because a sequence needs a p-value greater than 0.01 to pass, passing cumulative sum values (i.e., the "Expected Range") can be calculated using the formula provided in Section 3.1 of the NIST statistical test suite documentation.

Due to the rudimentary nature of the frequency test, further tests are required to assess the randomness of a given bit sequence. One such test is the longest run of ones in a block test. This test partitions a bit sequence into non-overlapping M-bit blocks, and determines the length of the longest consecutive run of '1' bits in each block. The run occurrences are counted, and the resulting distribution is compared with what would be expected from a random sequence. For the example shown in Figure 4b, a block size of M = 8 bits is used, and the bar heights and error bars in the figure represent the average and standard deviation of the results for the 56 bit sequences tested. The expected distribution for this test is simulated by performing the longest run of ones in a block test on 100,000 bits generated using the MATLAB randi function. A detailed overview of the longest run of ones in a block test and its p-value calculation can be found in Section 3.4 of the NIST statistical test suite documentation.

Deviations from the expected random distribution of longest run of ones would imply either an overall skew in the generated bits or that individual resolve steps may behave as correlated events. However, a balanced sequence that passes both the frequency and longest run of ones in a block test can still fail to be random if the output exhibits a bias for specific m-bit patterns. To test for this possibility, the serial test counts the frequency of all possible overlapping 2^m m-bit patterns in a sequence. The frequency distribution of m-bit patterns in a sequence is compared with the distribution of a random sequence. Because a random sequence should have no bias (i.e., every possible m-bit pattern has the same probability of occurrence), its frequency distribution is expected to be uniform. The expected count for each m-bit pattern in a random sequence is then calculated as $(n-m)/2^m$, where n represents the number of bits tested. Figure 4c illustrates the serial test for m = 4 bits for both our experimental bit stream and the expected uniform distribution of a random sequence. A detailed overview of the serial test and its p-value calculation can be found in Section 3.11 of the NIST statistical test suite documentation.

While the serial test can test for simple output non-uniformity, it may not detect larger periodic components in generated bit sequences. In order to test for periodic features, the discrete fast Fourier transform (FFT) test checks for non-uniformities in the frequency domain. Because a random bit sequence would be expected to have a uniform distribution of peak values, the FFT test determines whether 95% of the tested bit sequence peak values are below the 95% peak value threshold expected for a random bit sequence. If the percentage of tested bit sequence peak values below the 95% threshold significantly deviates from 95%, periodic components are likely to be present and the tested bit sequence is unlikely to be random. A detailed overview of the FFT test

and its p-value calculation can be found in Section 3.6 of the NIST statistical test suite documentation.

The full results of the NIST STS randomness tests are summarized in Table 3.2. In all cases, the post-processed bit stream is found to be random.[218] As an additional check, the post-processed bit stream was further examined and affirmed to be random by the Rabbit and Alphabit tests from the Test U01 software suite,[219] as can be seen in Table 3.3. Overall, these results show that appropriately designed and biased SWCNT SRAM cells produce highly random bit streams and thus serve as effective TRNGs.

Table 3.2 | Summary of NIST STS results

NIST statistical test[a]	p-value	proportion	result[b]
Frequency	0.007694	56/56	PASS
Block Frequency	0.350485	56/56	PASS
Cumulative Sums	0.153763	56/56	PASS
Runs	0.085587	53/56	PASS
Longest Run of Ones	0.935716	56/56	PASS
Rank	0.956003	1/1	PASS
Discrete Fourier Transform	0.002374	55/56	PASS
Approximate Entropy	0.236810	54/56	PASS
Serial	0.455937	56/56	PASS

[a] With the exception of the Rank test, these tests were performed using 56 sequences of 1,096 bits each, such that only the first 61,376 collected bits were tested.
[b] A p-value > 0.001 and a proportion > 53/56 are required for a test to pass.

Table 3.3 | Summary of TestU01 results

	Rabbit Battery Tests		Alphabit Battery Tests	
statistical test[a]	p-value[b]	result	p-value[b]	Result
MultinomialBitsOver	0.02	PASS	0.22	PASS
HammingIndep	0.06	PASS	0.25	PASS
HammingCorr	0.07	PASS	0.34	PASS
RandomWalk1	0.25	PASS	0.04	PASS
ClosePairsBitMatch	0.34	PASS	-	-
AppearanceSpacings	0.67	PASS	-	-
LinearComp	0.23	PASS	-	-
LempelZiv	0.97	PASS	-	-
Fourier1	0.90	PASS	-	-
Fourier3	0.10	PASS	-	-
PeriodsInStrings	0.10	PASS	-	-
HammingWeight	0.61	PASS	-	-
AutoCor	0.50	PASS	-	-
Run	0.28	PASS	-	-

[a]Collected bits are converted to 1,919 32-bit doubles in the range of [0,1) to match TestU01 statistical test input formats, such that only the first 61,408 collected bits are tested.
[b]For tests that are performed multiple times with different testing parameters, the lowest p-value is reported.

In conclusion, we have demonstrated a TRNG using SRAM cells based on solution-processed semiconducting SWCNTs. By appropriately biasing the SRAM cells into a metastable state, thermal noise fluctuations are digitized to generate random bit streams. The demonstrated bit generation and post-processing strategy can be readily implemented in hardware and requires minimal transistor and computational overhead. Furthermore, the randomness of the resulting bit stream was rigorously confirmed using a comprehensive panel of established statistical tests. By using solution-processed SWCNTs and circuit architectures that are compatible with large-scale manufacturing methods, this work provides a pathway for the development of low-cost, ultra-thin,

and mechanically flexible security devices that can be adopted in next-generation portable and wearable electronics.

Chapter 4: Carbon nanotube ohmic-contact-gated transistors

The growing demand for ubiquitous data collection has driven the development of sensing technologies based on flexible electronics. As a result, solution-processed semiconductors have been widely employed due to their flexibility and compatibility with low-cost manufacturing. However, to fully exploit their potential in emerging flexible electronics, high performance amplifiers based on these materials must be realized at scaled transistor dimensions. Here, we use atomically-thin, semiconducting, solution-processed single-walled carbon nanotubes to develop a novel ohmic-contact-gated transistor that enables output current saturation in short channel limits without compromising the output current drive. The ohmic-contact-gated transistors are used in common-source amplifiers to attain the highest output current density (~30 $\mu A \cdot \mu m^{-1}$) and length-scaled signal gain (~230 μm^{-1}) to date for amplifiers based on solution-processed semiconductors. The utility of these amplifiers for emerging sensing technologies is demonstrated by the amplification of complex analog biological signals. Furthermore, the fabrication design demonstrated in this work can be generalized to other semiconducting nanomaterials, establishing a promising route to high performance, solution-processed analog electronics.

4.1 Challenges in solution-processed short-channel amplifiers

The advent of robust artificial learning software has enabled the extraction of actionable insights from empirical and noisy sensory data available via personalized electronic gadgets[231,232]. Significantly improved computation power, communication bandwidth, and efficiency of these software classifiers has led to unprecedented levels of data collection from sensing hardware, such as wearable and Internet of Things (IoT) devices[233,234]. Owing to this growing demand for ubiquitous monitoring and data collection, tailored sensing technologies are being developed for

specific applications. One of these emerging applications is flexible electronic sensors[235-237], often used for sensing complex biological signals along bendable and moving surfaces. The use of conventional rigid semiconductors for these applications requires expensive processing, limiting their impact and integration[238]. As a result, solution-processed semiconductors have been employed in these applications due to their intrinsic mechanical flexibility and compatibility with low-cost manufacturing methods[239-242]. A critical component in these sensing applications is the small-signal amplifier, which increases the signal amplitude and drives subsequent analog-to-digital converters (ADCs). However, the utility of amplifiers based on solution-processed semiconductors within practical sensing systems is limited by their low output currents and transistor scaling limitations[243-246]. Therefore, solution-processed-based amplifiers with high performance at scaled transistor dimensions must be realized to fully exploit the potential of solution-processed materials in emerging flexible electronics.

Here, we introduce an ohmic-contact-gated transistor (OCGT), a novel transistor design that enables unprecedented levels of output current saturation in short channel limits (i.e., channel lengths < 300 nm) using atomically thin semiconductors without compromising the output current drive. We use solution-processed single-walled carbon nanotube (SWCNT) random networks to implement OCGTs that mitigate short channel effects to achieve low output conductance (~60 $nS \cdot \mu m^{-1}$) with high output current levels (~0.3 mA), overcoming the tradeoff relationship that is typically observed in conventional field-effect transistors (FETs). These SWCNT OCGTs are then used in common-source amplifiers to attain the highest output current density (~30 $\mu A \cdot \mu m^{-1}$) and length-scaled signal gain (~230 μm^{-1}) to date for amplifiers based on solution-processed semiconductors. The utility and robustness of these amplifiers is demonstrated by amplifying a

number of analog biological signals from sensors commonly found in IoT and medical devices, including an electromyography sensor, a photoplethysmogram sensor, and an accelerometer. Because the facile OCGT fabrication design can be generalized to other semiconducting nanomaterials, this work has wide-ranging implications for solution-processed analog electronics.

4.2 Fabrication of SWCNT OCGTs

OCGTs were fabricated using an optimized, self-aligned method compatible with conventional photolithography (Figure 4.1). First, a bottom gate electrode and gate oxide layer is defined on an undoped Si wafer, followed by the deposition of solution-processed SWCNTs with 99.9% semiconducting purity (Figure 4.1, step 1). Another step of photolithography and directional metal evaporation is used to define the bottom contact electrode (Figure 4.1, step 2). A conformal dielectric is grown using atomic layer deposition (ALD) prior to liftoff (Figure 4.1, step 3), resulting in a dielectric extending from the bottom contact due to the undercut of the negative photoresist (Figure 4.1, step 4; Figure 4.2). Lastly, the top contact electrode is patterned using photolithography and directional metal evaporation such that it fully overlaps the dielectric extending from the bottom contact (Figure 4.1, step 5).

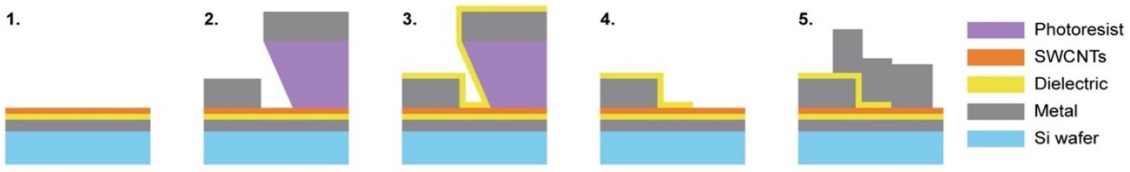

Figure 4.1 | SWCNT OCGT fabrication. Overview of OCGT fabrication using conventional photolithography. (1) A layer of semiconducting SWCNTs is placed on top of a bottom gate structure. (2) Negative photolithography and directional metal evaporation are used to deposit the bottom contact electrode. (3) A dielectric layer is conformally grown using ALD. (4) The

bottom contact electrode with a dielectric extension is defined following liftoff. (5) The overlapping top contact electrode is deposited using conventional photolithography and directional metal evaporation.

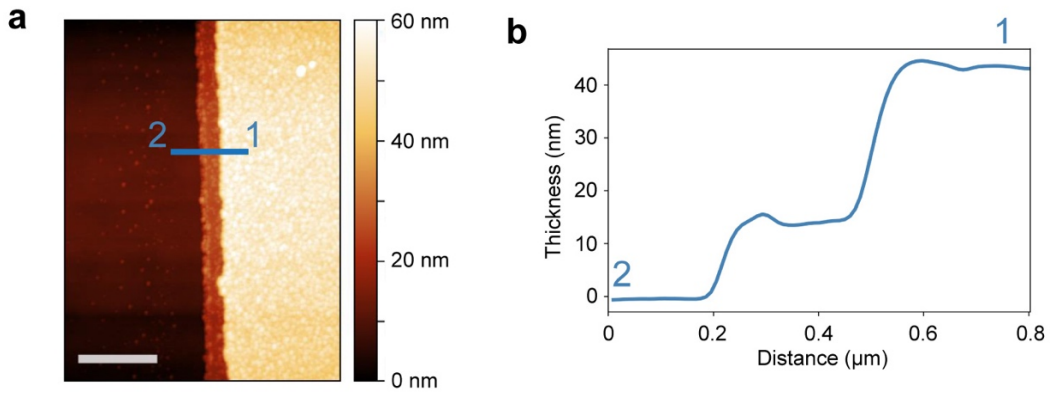

Figure 4.2 | Characterization of dielectric extension. a, AFM image of a dielectric extension following photolithography, metal evaporation, ALD growth and liftoff. The black line highlights the location of an AFM profile from (1) the metal-dielectric stack to (2) the substrate (1 μm scale bar). **b,** AFM thickness profile for the blue line in **a**. The length and thickness of the dielectric extension are approximately 280 nm and 12 nm, respectively.

The optical micrograph in Figure 4.3 shows the lateral layout of fully fabricated OCGTs. The intentional overlap of the dielectric extension with the top electrode determines the device channel length (L) and creates a secondary gate that is shorted to the top electrode. A 3D schematic of the OCGT device design in Figure 4.4 highlights how L is defined by the contact electrodes and the dielectric extension. The device layout and dielectric extension were designed such that the OCGT had a channel width (W) of 10 μm and L of 280 nm.

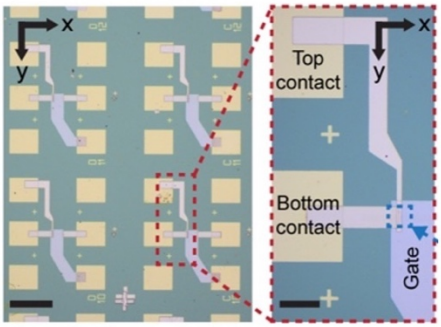

Figure 4.3 | SWCNT OCGT lateral view. Optical micrograph of multiple (left, 200 µm scale bar) and a single (right, 50 µm scale bar) OCGT device. Note that the small top contact metal electrode bar overlaps the bottom contact. X and Y coordinates are shown for clarity.

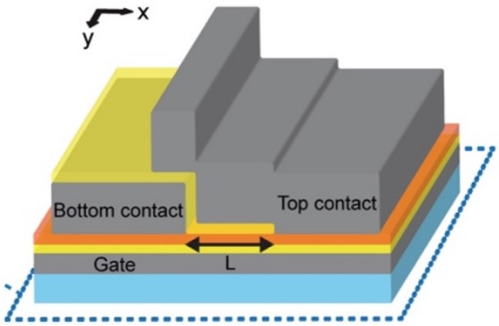

Figure 4.4 | SWCNT OCGT device schematic. Schematic of an OCGT device, highlighting the relative positions of the contact electrodes and the definition of the channel length (L) by the dielectric extension. X and Y coordinates are shown for clarity.

A thin high-k dielectric (12 nm HfO_2) and an ohmic contact metal (Pd) were used for optimal short-channel performance of the SWCNT channel[247-249]. Where appropriate, Al was used in the electrode metal stack to seed subsequent ALD dielectric growth. Artificially shifting of the layers of a SWCNT OCGT along the y-direction to reveal the underlying structure and described materials selection is shown in Figure 4.5, along with an atomic force microscopy (AFM) image of the SWCNT random network with a linear density of ~40 CNTs·µm^{-1}. A detailed overview of the SWCNT OCGT fabrication methods is found below.

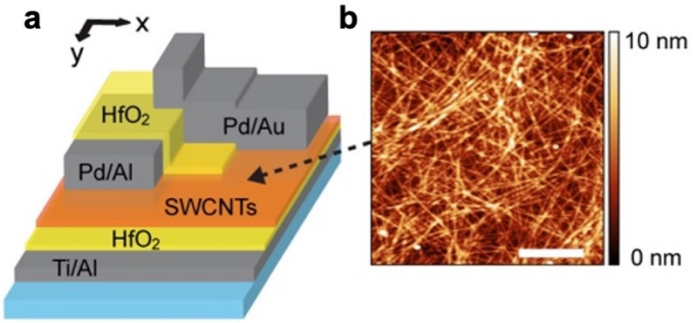

Figure 4.5 | SWCNT OCGT materials selection. a, Layered schematic of the fabricated SWCNT OCGT device using 12 nm HfO_2 dielectric layers, Pd ohmic contacts, and a SWCNT random network with ultrahigh (i.e., 99.9%) semiconducting purity. X and Y coordinates are shown for clarity. **b,** AFM image of the SWCNT network with a linear density of ~40 CNTs·μm^{-1} (500 nm scale bar).

SWCNT OCGTs were fabricated on an undoped Si wafer with a 300 nm thermal oxide. The role of the thermal oxide is to enable optical contrast in atomically thin semiconductors. Negative photolithography, thermal evaporation (10 nm of Cr, then 50 nm of Au), and liftoff in acetone were used to define contact pads. Negative photolithography and e-beam evaporation (5 nm of Ti, then 15 nm of Al) were used to deposit patterned gate electrodes. Directly following e-beam evaporation, a conformal HfO_2 (12 nm) gate dielectric was grown via ALD using tetrakis(dimethylamido)hafnium(IV) (TDMAH) and water at 100° C (Savannah S100, Cambridge NanoTech). Liftoff was then performed in Remover PG (MicroChem) heated to 80° C. The substrates were treated with reactive ion etching (RIE) in an O_2 plasma atmosphere (100 W, 4 Pa, 2 min, 10 s.c.c.m. of O_2), a 5 min dip in poly-L-lysine solution (0.1% w/v in water, Sigma-Aldrich P8920), and a gentle rinse in DI water. Ultrahigh purity (99.9% semiconducting) SWCNTs were deposited in this modified surface by dipping the substrates in IsoSol-S100 (NanoIntegris) solution, followed by a gentle rinse with 5 mL of toluene to remove excess material. The substrates

were then annealed at 200° C in ambient, followed by cleaning with acetone and IPA. Positive photolithography, RIE in an O_2 plasma atmosphere (100 W, 26.5 Pa, 15 sec, 20 s.c.c.m. of O_2), and liftoff in acetone were used to define the SWCNT channel. Negative photolithography, e-beam evaporation (40 nm of Pd, then 10 nm of Al), HfO_2 (12 nm) deposition via ALD and liftoff in heated Remover PG (MicroChem, Inc.) were again used to define the patterned bottom contact electrodes with a dielectric extension due to the photoresist undercut. The length of this dielectric extension was controlled by changing the development time of the negative photoresist, and its length was characterized using AFM. Negative photolithography, e-beam evaporation (70 nm of Pd, then 5 nm of Au) and liftoff in acetone were used to define the patterned top contact electrode such that it overlapped the dielectric extension of the bottom contact electrode.

The OCGT geometry provides a key advantage by gating the semiconducting channel with both the bottom gate and top contact electrode without the need of additional terminals beyond the conventional gate-source-drain configuration. While this contact-gating can be accomplished by other devices, such as source-gated transistors[250,251], these devices rely on Schottky barrier contacts in 2D materials[252] and/or a vertical depletion regions in thicker semiconductors (organic or inorganic) which are not compatible with short-channel scaling[253-255]. In contrast, the presented OCGT geometry utilizes ohmic contact with a short-channel length to achieve contact-gating with superior device performance. The OCGT fabrication design also provides a number of key advantages when compared with conventional source-gating schemes. In particular, the use of a dielectric extension to define L allows for the high-throughput fabrication of short-channel devices in sub-diffraction limits using standard photolithography systems. Additionally, the robust

fabrication design can be extended to other atomically thin nanomaterials and van der Waals heterojunctions.

4.3 Performance of SWCNT OCGTs

The electronic transport of the SWCNT OCGTs was measured in ambient conditions under two distinct modes of operation. In one mode, the bottom contact is at the supply voltage (V_{DD}) while the top contact, which overlaps the semiconducting channel and bottom contact, is grounded. Conversely, in the second mode of operation the bottom contact is grounded while the overlapping top contact is at V_{DD}. Unlike conventional FETs, this switch in drain-source biasing polarity leads to significant changes in output and transfer characteristics of OCGTs. This is due to the intrinsic electrostatic asymmetry rising from asymmetric geometry of the contacts of OCGTs, where the field effects in the channel are controlled by both the bottom gate and the overlapping top contact. The transfer and output characteristics under these two modes of operation were collected for 67 OCGTs. The behavior of a prototypical OCGT is discussed below and shown in Figures 4.6, 7,10,12,14 and 15 for clarity. A detailed overview of OCGT device testing can be found below.

The output, transfer, and leakage characteristics of fabricated OCGTs were measured using a Cascade Microtech Summit 12000 semi-automatic ambient probe station with a Keithley 4200-SCS system. Data was collected using the a custom Keithley 4200 test module. Data analysis was performed using custom MATLAB and python scripts.

The transfer characteristics (I_{DS}–V_{GS}) of the SWCNT OCGTs are measured by sweeping the gate-source voltage (V_{GS}) while changing the drain-source voltage (V_{DS}). The linear and log-linear transfer characteristics of a prototypical device are shown in Figure 4.6 and Figure 4.7,

respectively, for both modes of operation described above (i.e., top contact at ground and top contact at V_{DD}).

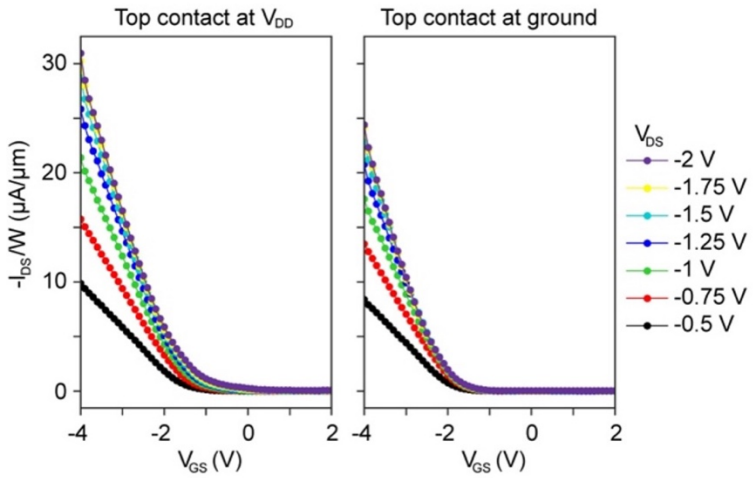

Figure 4.6 | Performance of a SWCNT OCGT – Linear transfer. Linear transfer characteristic (I_{DS} –V_{GS}) where V_{DS} is varied from -0.5 V to -2 V in -0.25 V steps. The transfer characteristic results are shown for OCGTs operating in two modes: with their top contact at V_{DD} (left) and ground (right).

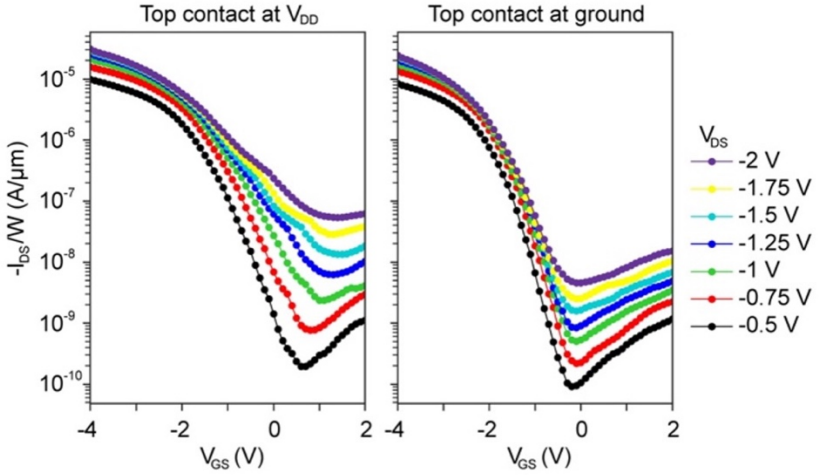

Figure 4.7 | Performance of a SWCNT OCGT – Log-linear transfer. Log-linear transfer characteristic (I_{DS} –V_{GS}) where V_{DS} is varied from -0.5 V to -2 V in -0.25 V steps. The transfer characteristic results are shown for OCGTs operating in two modes: with their top contact at V_{DD} (left) and ground (right).

The use of ultrahigh purity semiconducting SWCNTs and ultrathin high-k dielectric layers provides improved electrostatic control of the channel, resulting in unipolar p-type transport with a simultaneous high I_{on}/I_{off} ratio ($>10^4$), high current density (~10 $\mu A \cdot \mu m^{-1}$), and negligible leakage current (~10 $pA \cdot \mu m^{-1}$) despite the short length of the channel ($L < 300$ nm). While in conventional FETs the I_{on}/I_{off} ratio decreases with increasing current output (i.e., increasing $|V_{DS}|$), this deleterious effect is mitigated in OCGTs when the top contact at ground. At low values of $|V_{DS}|$ (-0.5 V), the difference between the modes of operation for both $\log(I_{on}/I_{off})$ and $|I_{on}|/W$ is minimal (i.e., the median $\log(I_{on}/I_{off})$ is 4.5 and 4.4, and the median $|I_{on}|/W$ is 13 and 14 $\mu A \cdot \mu m^{-1}$ for the top contact at ground and the top contact at V_{DD}, respectively). However, at a high $|V_{DS}|$ (-2 V), there is a significant improvement in the I_{on}/I_{off} ratio when the top contact is at ground with only a small loss in $|I_{on}|/W$ (i.e., the median $\log(I_{on}/I_{off})$ is 3.1 and 2.6, and the median $|I_{on}|/W$ is 39 and 44 $\mu A \cdot \mu m^{-1}$ for the top contact at ground and the top contact at V_{DD}, respectively; Figure 4.8 and 4.9). This improvement in I_{on}/I_{off} ratio increases with increasing $|V_{DS}|$, providing a key advantage over conventional FET designs.

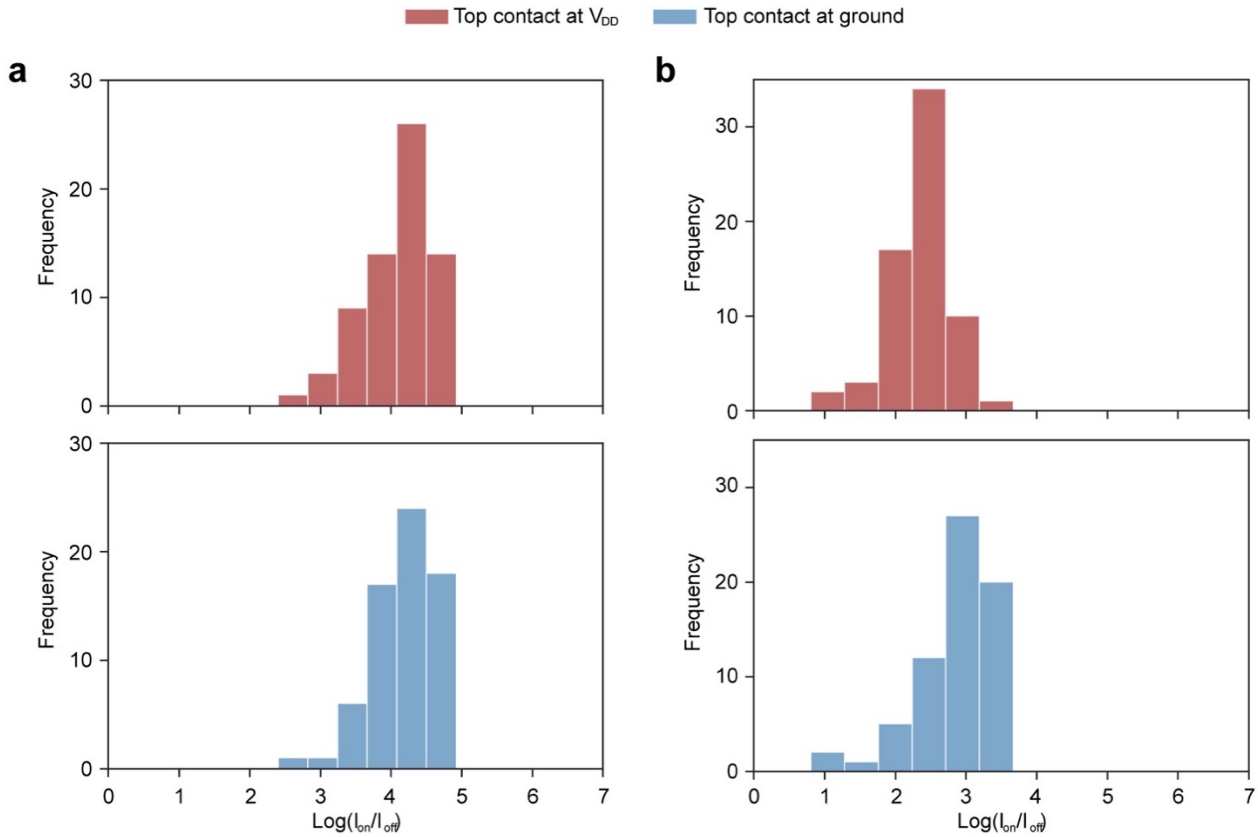

Figure 4.8 | Histogram of SWCNT OCGT ON/OFF ratio performance. a,b, Histogram of Log(I_{on}/I_{off}) values for (**a**) V_{DS} = -0.5 V and (**b**) V_{DS} = -2 V. These characterization results are shown for 67 OCGT devices when the top contact is at V_{DD} (red) and ground (blue).

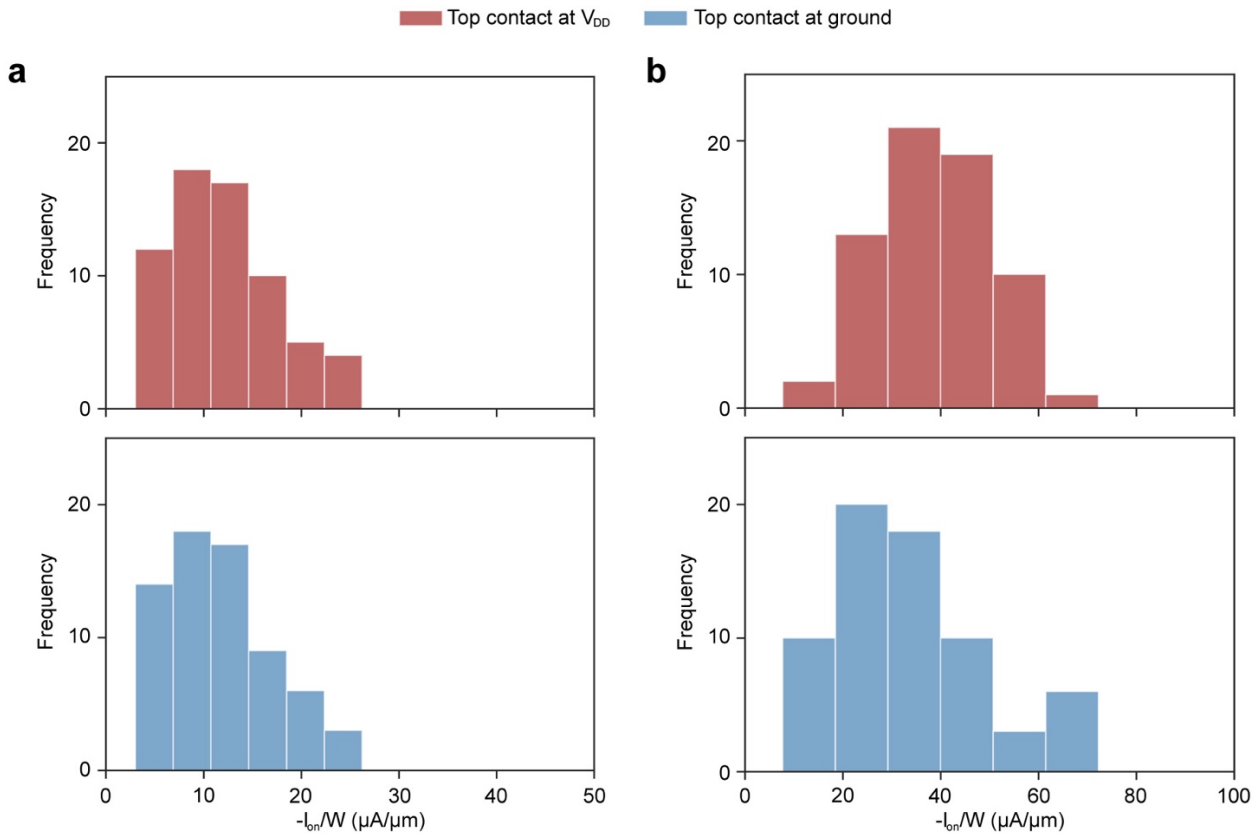

Figure 4.9 | Histogram of SWCNT OCGT on-current performance. a,b, Histogram of on-current density (I_{on}/W) values for (**a**) V_{DS} = -0.5 V and (**b**) V_{DS} = -2 V. These characterization results are shown for 67 OCGT devices when the top contact is at V_{DD} (red) and ground (blue).

The output characteristics (I_{DS}–V_{DS}) of the SWCNT OCGTs are measured by sweeping V_{DS} while changing V_{GS}. The linear output characteristics of a prototypical device in both modes of operation are shown in Figure 4.10. The use of ohmic contacts (i.e., Pd) and high density SWCNT channels results in high output currents, such that at a high $|V_{GS}|$ (-4 V), the OCGTs exhibit a median maximum output current density ($|I_{DS,max}|/W$) of 29 and 33 $\mu A \cdot \mu m^{-1}$ for the top contact at ground and the top contact at V_{DD}, respectively (Figure 4.11). Most notably, at high $|V_{GS}|$ biases with the top contact at ground, SWCNT OCGTs achieve output current saturation concurrently with high output currents despite the short channel length. This is in sharp contrast

with published short-channel SWCNT FETs, where output current saturation is either limited to overall low currents[249,256,257] or the current saturation regime is not realized at all[258-260]. Additionally, output current saturation is achieved despite the use of SWCNT high density random networks that are known for deleterious electrostatic screening of the applied gate field[261]. These results highlight how the OCGT contact geometry can reduce short-channel effects, including channel-length modulation[262].

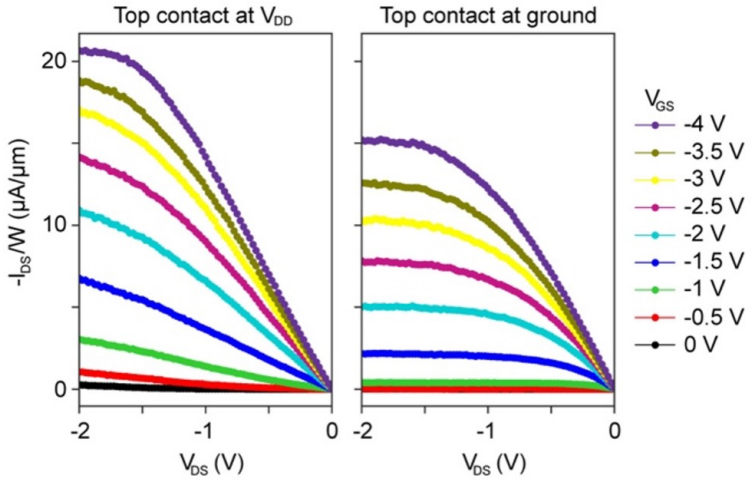

Figure 4.10 | Performance of a SWCNT OCGT – Linear output. Linear output characteristic (I_{DS} –V_{DS}) where V_{GS} is varied from 0 V to -4 V in -0.5 V steps. The output characteristic results are shown for OCGTs operating in two modes: with their top contact at V_{DD} (left) and ground (right).

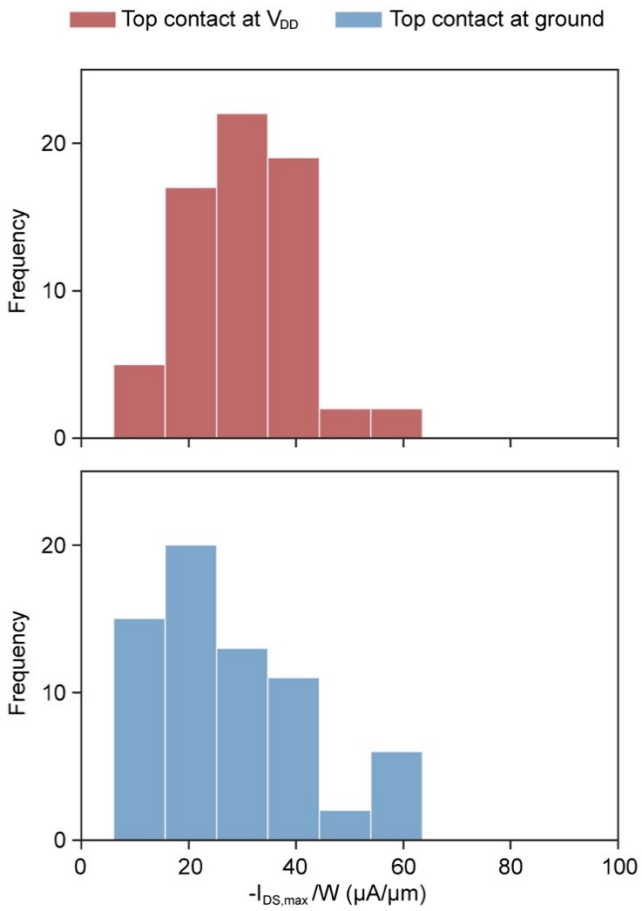

Figure 4.11 | Histogram of SWCNT OCGT maximum output current performance. Histogram of maximum output current density ($I_{DS,max}/W$) values for V_{GS} = -4 V. These characterization results are shown for 67 OCGT devices when the top contact is at V_{DD} (red) and ground (blue).

These advantages are manifested in two key transistor metrics: transconductance (i.e., g_m, where $g_m = dI_{DS}/dV_{GS}$ at a fixed V_{DS}) and output conductance (i.e., g_o, where $g_o = r_o^{-1} = dI_{DS}/dV_{DS}$ at a fixed V_{GS}, where r_o is the output resistance). Figure 4.12 shows the log-linear behavior of width normalized g_m as a function of V_{GS} at V_{DS} = -2 V and width normalized g_o as a function of V_{DS} at V_{GS} = -1 V for a prototypical device in both modes of operation. The maximum g_m is similar for

both modes of operation (i.e., the median maximum g_m/W is 31 $\mu S \cdot \mu m^{-1}$ for both the top contact at ground and the top contact at V_{DD}; Figure 4.13a).

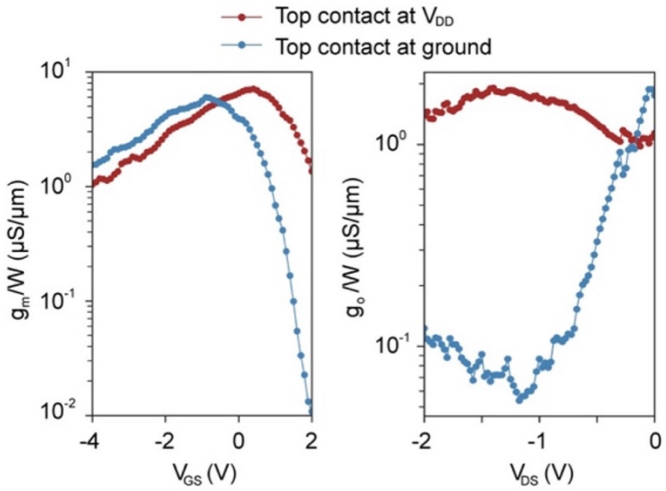

Figure 4.12 | Performance of a SWCNT OCGT – transconductance and output conductance. Log-linear behavior for width-normalized transconductance g_m/W (left) and width-normalized output conductance g_o/W (right) at V_{DS} = -2 V and V_{GS} = -1V, respectively, when the top contact is at V_{DD} (red) and ground (blue).

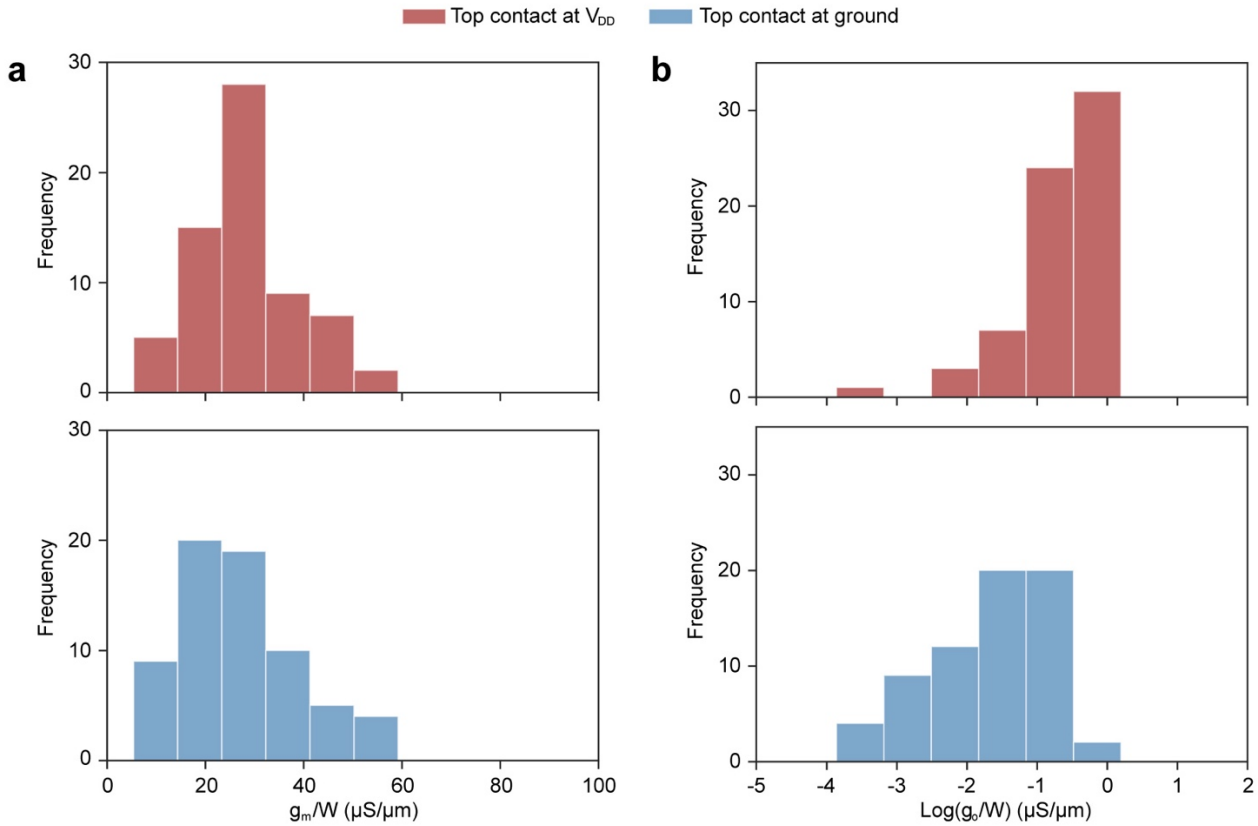

Figure 4.13 | Histogram of SWCNT OCGT output conductance and transconductance performance. a, Histogram of width-normalized transconductance (g_m/W) values at V_{DS} = -2 V. **b,** Histogram of width-normalized output conductance (g_o/W) values at V_{GS} = -1 V. The logarithmic values are given for improved clarity. These characterization results are shown for 67 OCGT devices when the top contact is at V_{DD} (red) and ground (blue).

However, g_o is significantly improved due to saturation of the output current such that, at high output currents (i.e., high $|V_{DS}|$), g_o is decreased by an order of magnitude when the top contact is at ground (i.e., the median g_o/W is 60 and 670 nS·μm^{-1} for the top contact at ground and the top contact at $V_{DD,}$ respectively; Figure 4.13b). This improvement in g_o with minimal compromise of g_m (Figures 4.14 and 4.15) highlights the potential for using OCGTs in scaled flexible analog circuit applications beyond standard photolithography limits. For a summary of key SWCNT OCGT performance metrics described above, see Table 4.1.

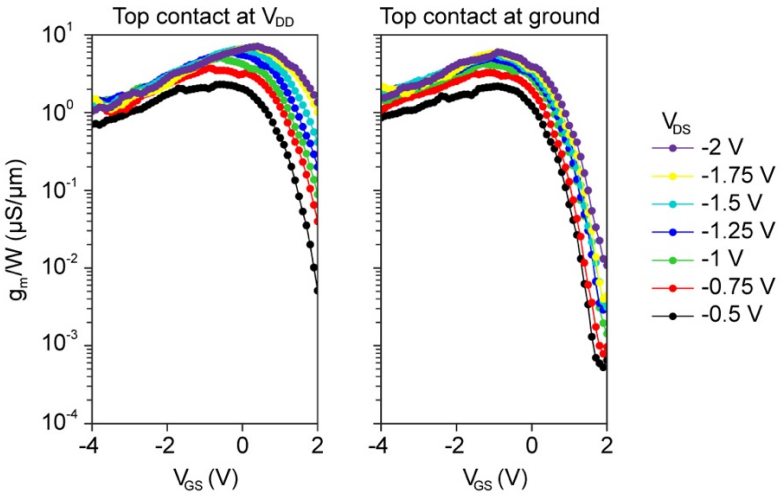

Figure 4.14 | SWCNT OCGT transconductance characterization. Log-linear behavior for width-normalized transconductance (g_m/W) when V_{DS} is varied from -0.5 V to -2 V in -0.25 V steps. These characterization results are shown for a prototypical OCGT device when the top contact is at V_{DD} (left) and ground (right).

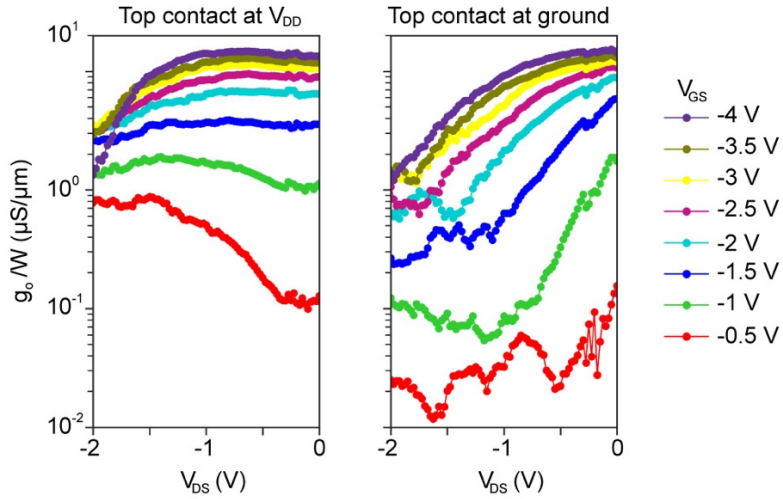

Figure 4.15 | SWCNT OCGT output conductance characterization. Log-linear behavior for width-normalized output conductance (g_o/W) when V_{GS} is varied from -0.5 V to -4 V in -0.5 V steps. These characterization results are shown for a prototypical OCGT device when the top contact is at V_{DD} (left) and ground (right).

Table 4.1 | Median values of key performance metrics for 67 SWCNT OCGTs

	Top contact bias

	Metric	Bias	V_{DD}	Ground
Transfer characteristic	$Log(I_{on}/I_{off})$	V_{DS} = -0.5 V	4.4	4.5
		V_{DS} = -2 V	2.6	3.1
	I_{on}/W	V_{DS} = -0.5 V	-14 $\mu A \cdot \mu m^{-1}$	-13 $\mu A \cdot \mu m^{-1}$
		V_{DS} = -2 V	-44 $\mu A \cdot \mu m^{-1}$	-39 $\mu A \cdot \mu m^{-1}$
	g_m/W	V_{DS} = -2 V	31 $\mu S \cdot \mu m^{-1}$	31 $\mu S \cdot \mu m^{-1}$
Output characteristic	$I_{DS,max}/W$	V_{GS} = -4 V	-33 $\mu A \cdot \mu m^{-1}$	-29 $\mu A \cdot \mu m^{-1}$
	g_o/W	V_{GS} = -1 V	670 $nS \cdot \mu m^{-1}$	60 $nS \cdot \mu m^{-1}$

Note, the present OCGTs operate in a distinct fashion when compared to source-gated transistors based on inorganic and organic semiconductor thin films. Conventional source-gated transistors rely on creation of an extended depletion region under the contacts that completely blocks carrier injection at higher biases, resulting in superior current saturation at smaller biases but at the expense of the overall current density[245,254,255]. Thus, conventional source-gating concepts rely on the finite thickness of the semiconductors. Additionally, a recent demonstration of source-gating using overlapping electrodes in monolayer semiconductor (MoS_2) transistors likely involved Schottky contacts which limited output current density[252]. Because the OCGTs presented here rely exclusively on electrostatic control of the channel, the resulting devices show simultaneous improvements in competing device metrics.

4.4 SWCNT OCGT-based amplifiers for practical sensing systems

The novel electrostatics in SWCNT OCGTs enable significant improvements in transistor metrics, namely, g_m and g_o which are key metrics in small-signal amplifiers for signal acquisition systems[263,264]. A typical signal acquisition process is illustrated in Figure 4.16, where the small analog signal is amplified, converted to a digital signal, and then processed into a digital output.

Small-signal amplifiers play a critical role in the acquisition of low-amplitude sensory data since they drive the subsequent ADC components and increase the signal amplitude to appropriate levels for analog signal digitization[265]. Therefore, practical sensing systems require amplifiers with both high signal gain and high current output.

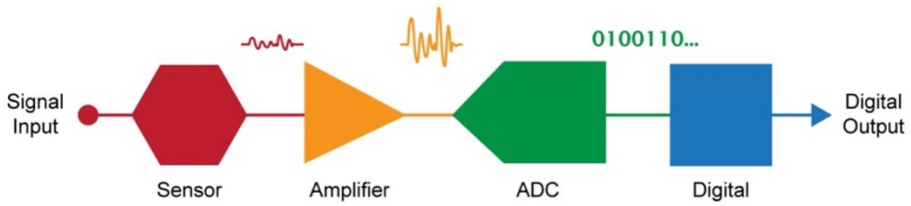

Figure 4.16 | Signal acquisition overview. Overview of common signal acquisition systems, where sensors acquire analog signals (red) that are amplified (yellow), digitized (green), and processed digitally (blue), resulting in a digital output.

Solution-processed semiconductors have been employed in emerging sensing systems due to their potential for low-cost, flexible electronics[240,241]. However, amplifiers based on these materials suffer from low output currents and transistor scaling limitations[243,245]. As a result, these emerging sensing systems would benefit from amplifiers based on solution-processed semiconductors that achieve high current densities (i.e., $|I_{DS}|/W$) and high signal gain at scaled dimensions (i.e., gain/L). The performance of OCGTs in these key metrics is characterized by using them in a single-stage, single-transistor common-source amplifier (Figure 4.17). Common-source amplifiers have a small voltage signal at the transistor gate (V_{IN}) that is amplified (V_{OUT}) with a gain of $V_{OUT}/V_{IN} \sim -g_m/g_o$. Common source amplifiers are ideal for the small input signals in solution-processed sensing systems due to their high input impedance resulting from dielectrics with negligible leakage. The signal gain of OCGT-based common source amplifiers is quantified

by applying a small sinusoidal input signal V_{IN} at the gate input that produces an inverted output signal V_{OUT}.

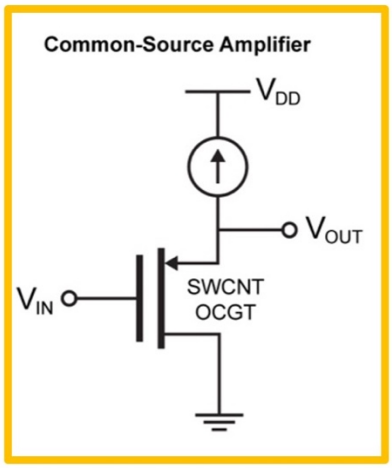

Figure 4.17 | SWCNT OCGT-based amplifier. Circuit diagram for an SWCNT OCGT-based common-source amplifier, where a small input signal (V_{IN}) is amplified (V_{OUT}) by a gain proportional to g_m/g_o.

The amplified output V_{OUT} is characterized for both modes of operation of the OCGT, where a substantial improvement in gain is expected when the top contact is at ground due to ten-fold lower g_o compared to when the top contact is at V_{DD}. As shown in Figure 4.18, a sinusoidal V_{IN} with an amplitude of 5 mV is amplified with a gain of ~5 and ~68 when the top contact is at V_{DD} and the top contact is at ground, respectively. This increase in signal gain highlights the advantages of the OCGT geometry, where a high signal gain and high current density can be achieved at short-channel lengths.

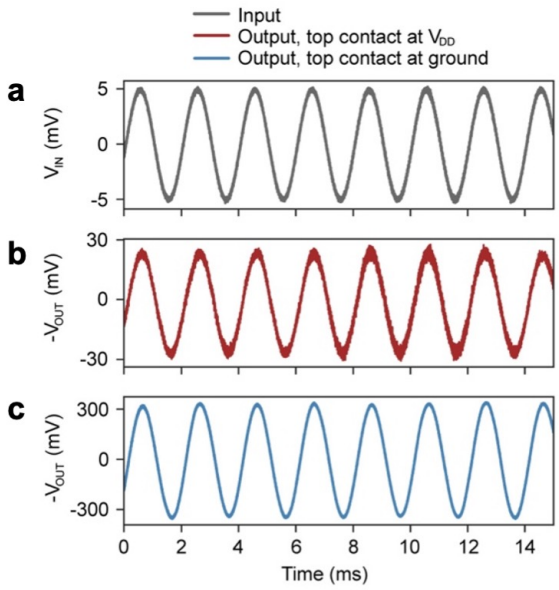

Figure 4.18 | Characterization of signal gain in SWCNT OCGT-based amplifier. Characterization of SWCNT OCGT amplifier where the signal gain (V_{OUT}/V_{IN}) of a small sinusoidal signal (**a**) changes from ~ 5 (**b**) to ~ 68 (**c**) based on the top contact bias due to the order of magnitude change in g_o.

To further illustrate this point, Figure 4.19 shows a scatter plot of current density ($|I_{DS}|/W$) and length-scaled signal gain (gain/L) values for the best previously reported solution-processed amplifiers in literature. As shown, OCGT-based amplifiers (Figure 4.19, red star) outperform the best amplifier by over one and two orders of magnitude in length-scaled signal gain and current density, respectively. A detailed overview of OCGT-based amplifier testing is found below.

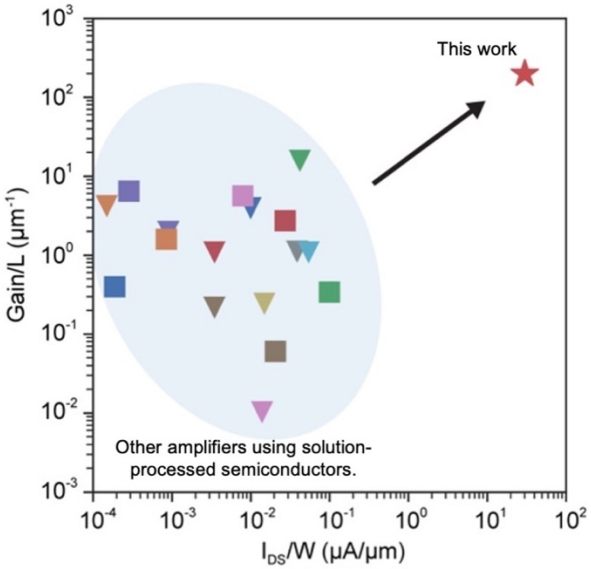

Figure 4.19 | Performance of amplifiers based on solution-processed semiconductors. Comparison of current density (I_{DS}/W) and length-scaled signal gain (Gain/L) values for the best previously reported solution-processed amplifiers[243-245,266-279]. This work (red star) outperforms the average solution-processed device by over two orders of magnitude in both metrics, and current state-of-the-art by over an order of magnitude in both metrics.

Amplifier measurements were performed using the Cascade Microtech Summit 12000 semi-automatic ambient probe station, a Keithley 2400 unit (current source and voltage supply), an Agilent 33500B waveform generator (input voltage signal), and a Tektronix TBS 2104 digital oscilloscope (input/output voltage measurement). The Keithley 2400 unit was operated as a current source at an output current of -30 μA with a maximum V_{DD} of -2.5 V. All circuit components were connected through a custom breadboard. Sinusoidal input signals were generated using the waveform generator's native software. Custom signals (i.e., electromyography, photoplethysmogram, and accelerator) were imported and generated using the waveform generator's arbitrary signal function. Accelerator input signal data was collected from the x-axis output of a SparkFun Triple Axis Accelerometer (ADXL335) attached to a waving hand.

Electromyography[280,281] and photoplethysmogram[282,283] input signal data were collected from online databases. Output voltage signal data was collected using the digital oscilloscope, and the data was then analyzed using custom python scripts.

To further demonstrate the practicality of OCGT-based amplifiers in solution-processed sensing systems, the signal gain from complex analog signals is characterized. Three raw sensor signals from common consumer and medical-grade wearable devices are used. The first signal is an enveloped electromyography (EMG) signal which measures electrical activity at the surface of a muscle[280,281] and is commonly used in the assessment of muscle and motor neuron health (Figure 4.20)[284].

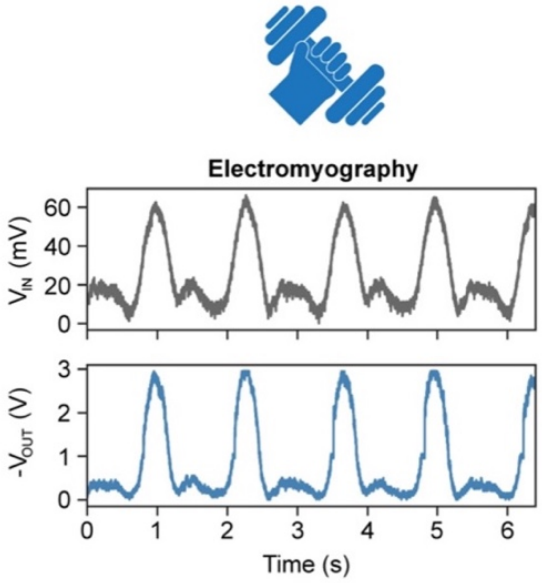

Figure 4.20 | Amplification of EMG sensor signal. Characterization of signal gain for a complex analog signal using SWCNT OCGT-based common-source amplifiers. The input (top) and output (bottom) voltages are shown for the amplification of a signal from an electromyography sensor[280,281]. The DC offsets of signals presented are modified for improved clarity.

The second signal is a photoplethysmogram (PPG) signal which measures blood volume changes[282,283] and is commonly used in heart rate monitoring (Figure 4.21)[285]. The third signal is

an accelerometer signal which is commonly used for monitoring physical activity (Figure 4.22)[286]. Beyond their unique shape, these signals range in amplitude from 10 – 60 mV and frequency from 0.5 – 5 Hz. As can be seen in Fig. 4a-c, the signal gains from these biologically relevant signals range from 50 – 60. The magnitude of signal gain in these measurements agrees with the common-source amplifier characterization detailed in Figure 4.18, and demonstrates the potential for SWCNT OCGT-based amplifiers in emerging sensing technologies. Furthermore, the fabrication design of OCGT devices can be applied to other thin semiconducting materials, providing a pathway to high performance analog electronics based on solution-processed semiconductors.

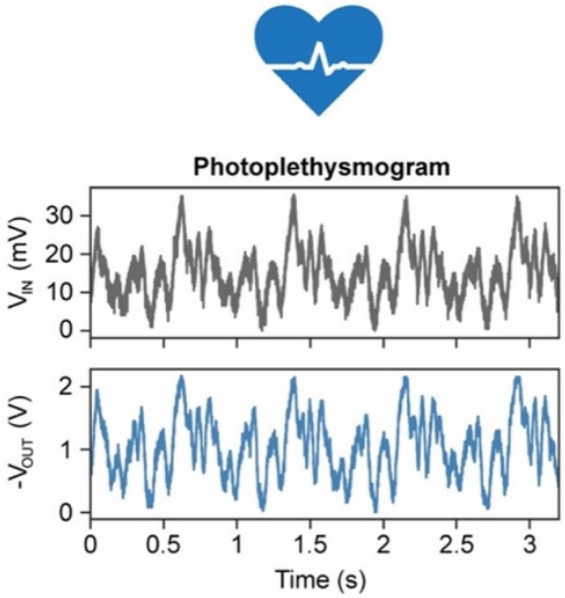

Figure 4.21 | Amplification of PPG sensor signal. Characterization of signal gain for a complex analog signal using SWCNT OCGT-based common-source amplifiers. The input (top) and output (bottom) voltages are shown for the amplification of a signal from a photoplethysmogram sensor[282,283]. The DC offsets of signals presented are modified for improved clarity.

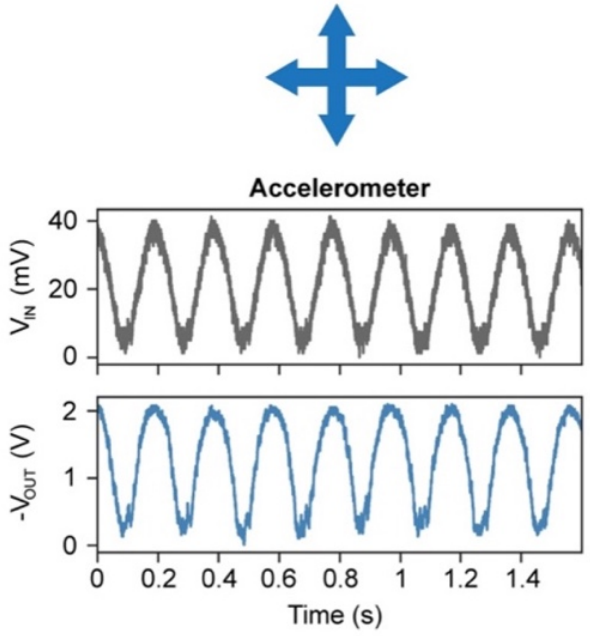

Figure 4.22 | Amplification of accelerometer sensor signal. Characterization of signal gain for a complex analog signal using SWCNT OCGT-based common-source amplifiers. The input (top) and output (bottom) voltages are shown for the amplification of a signal from an accelerometer. The DC offsets of signals presented are modified for improved clarity.

We have demonstrated that the novel OCGT fabrication design enables transistors with short-channel current saturation at high output currents when using solution-processed SWCNTs with ultrahigh semiconducting purity. Since the existing transistor tradeoffs of current saturation and output current can limit analog applications, we demonstrate the robustness of OCGTs against short-channel (i.e., L < 300 nm) effects by demonstrating an OCGT-based common-source amplifier. Among all amplifiers based on solution-processed semiconductors, common source amplifiers using SWCNT OCGTs achieve the highest reported length-scaled signal gain (~230 μm^{-1}) and the highest reported output current density (~30 $\mu A \cdot \mu m^{-1}$) to date. Furthermore, we demonstrate the utility of these amplifiers in practical sensing and health monitoring technologies by using them to amplify complex and small analog signals commonly recorded in medical and

consumer wearable devices. Thus, the fabricated SWCNT OCGTs in this work can be used to create digital and analog devices that can be readily integrated in emerging flexible electronics. Additionally, the demonstrated OCGT fabrication design can be used with other thin semiconducting materials, such that this work also establishes a route towards high performance solution-processed analog electronics.

Chapter 5: Conclusion and Outlook

5.1 Summary

With the growing adoption of traditional and mobile computing electronics, there is an increasing demand for high-performance electronic devices that are functionally compatible (e.g. low power, low cost, flexible) with next-generation technologies. Due to their small size, solution-processability, chemical stability, and superlative electronic properties, semiconducting single-walled carbon nanotubes offer a number of unique advantages and are functionally compatible with these complex requirements. To this end, the work presented in this thesis focuses on the development of materials processing methods and their impact on SWCNT device properties. With this understanding of processing-property relationships, this thesis demonstrates SWCNT devices with novel function and performance in two key applications, overcoming fundamental challenges in the development SWCNT-based security and sensing technologies.

First, innovative materials processing and device operation led to the development of the first true random number generator, overcoming a key application-specific challenge to low cost, flexible security electronics by demonstrating a ubiquitous security primitive using a solution-processed semiconductor. Second, further innovative transistor design and understanding of material processing-property relationships led to the development of a novel SWCNT OCGTs. This novel transistor design enables unprecedented levels of output current saturation in short channel limits without compromising the output current drive, overcoming the tradeoff relationship that is typically observed in conventional field-effect transistors FETs. These SWCNT OCGTs are then used in common-source amplifiers to attain the highest output current density and length-scaled signal gain to date for amplifiers based on solution-processed semiconductors, overcoming a key challenge in the development of practical sensing technologies.

The core innovations in materials processing, device operation and transistor design developed in this thesis work can be extended to other areas of SWCNT electronics. In particular, two of the most high-impact opportunities and their challenges are identified below in Sections 5.2 and 5.3. To conclude, Section 5.4 presents an overview of opportunities and challenges for the entire field of SWCNT electronics, and delineates a research roadmap for future SWCNT computational devices.

5.2 Synaptic transistors for neuromorphic computing

As previously discussed in Section 2.1.4, an emerging high-impact application of SWCNTs and other material systems is the development of hardware that supports neuromorphic computing architectures. In particular, the development of neuromorphic devices capable of imitating biological neural functions (e.g. depression, potentiation, long-term retention) is key in the realization of these architectures. To this end, this section describes a project in progress: synaptic transistors for neuromorphic computing based on solution-processed s-SWCNTs.

The synaptic transistor design and material selection are illustrated in the schematic on Figure 5.1a. This three-terminal device utilizes best practices developed in this thesis for materials processing and transistor design. Namely, the synaptic transistor utilizes (1) ultrahigh purity (99.9%) semiconducting SWCNTs networks (linear density ~15 CNTs·μm^{-1}) optimized for high performance, (2) optimized Pd contacts to minimize contact resistance effects, (3) a dielectric extension at the drain/source contacts to minimize modulation of the contact barrier by mobile ionic impurities, and (4) a W/L transistor ratio (i.e., 25/5 in μm) optimized for percolating SWCNT networks.

These transistors were inspired by work in electrolyte-gated transistors, where mobile ionic impurities caused hysteresis in the transfer characteristic of transistors using polyvinyl alcohol (PVA) dielectrics.[287] Similarly, we utilize a coating of PVA printed over the channel of bottom-gated SWCNT transistors to achieve the memristive behavior shown in Figure 5.1b. These synaptic devices demonstrated a switching ratio (i.e., difference between high-resistance and low-resistance state in hysteresis of the output curve) of ~10^3, and 10-fold lower operating voltages when compared with MoS_2 memtransistors.[288,289] Additionally, these synaptic transistors demonstrated long-term retention of memristive states with cycling endurances of over 1000 cycles.

Initial work on further exploring the nature of this memristive behavior showed that the stability of the high and low resistance states could be controlled through tuning of the Na ions in the printed PVA. More specifically, increasing the concentration of Na ions by adding sodium acetate to the printed PVA increased the stability of the output hysteresis. However, this results in a screening effect by the mobile ionic impurities, decreasing electrostatic coupling between the gate electrode and the SWCNT channel. Furthermore, commercially available PVA contains an unknown quantity of Na^+ impurities, presenting significant challenges in the detailed characterization Na^+ ion migration and reproducibility of synaptic behavior. Current work is exploring the use of tailored hexagonal boron nitride (hBN) ion gels as a replacement for PVA due to their chemical/mechanical/thermal stability, high ionic conductivities and ability to precisely control Na^+ ion concentrations through solution-processing.[290]

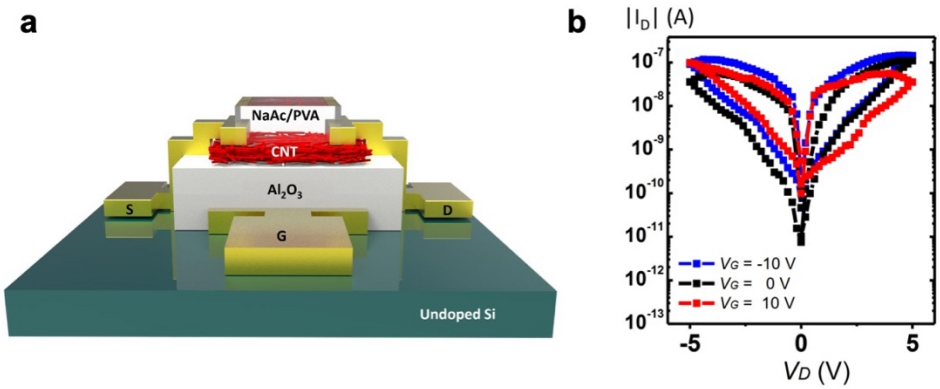

Figure 5.1 | SWCNT Synaptic transistor. a, Schematic of SWCNT synaptic transistor utilizing a bottom-gate geometry, a solution-processed SWCNT network channel and a printed PVA coating with added sodium acetate. **b,** Output characteristic for a SWCNT synaptic transistor with sodium acetate loading percentage of 1% at various gate voltages (blue, black, red). This output characteristic shows hysteresis with high-resistance and low-resistance state typical of memristive devices. Figures courtesy of Justin Qian.

Neuromorphic computing encompasses a wide range of solutions that merge both hardware and software innovations. Therefore, software simulations of how neuromorphic hardware would perform when implemented are needed to fully assess the impact of hardware-level innovations. To this end, this thesis work has developed software simulations of how synaptic transistors would perform in artificial learning tasks. More precisely, the software simulates unsupervised learning of how synaptic transistors being used to store synaptic weights would perform in the recognition of hand-written digits from the MNIST data set using a spiking neural network (SNN) and a simplified spike-timing-dependent plasticity (STDP) learning scheme. As shown in Figure 5.2a, the two-layer neural network can be implemented in hardware using a conventional crossbar architecture where the synaptic weights at the crossbar intersection are the synaptic devices being assessed. Using the simplified STDP rule illustrated in Figure 5.2b, output neurons can be trained in artificial image recognition with significantly less computational overhead than conventional

software implementations. For conventional memristive devices, the trained output neurons (Figure 5.3a) can achieve recognition rate (i.e., accuracy) as high as 94% (Figure 5.4b), providing a target of performance for any future neuromorphic devices. With this, we can use these software simulations for validation of neuromorphic devices fabricated, as well as a tool for quantitative feedback that can help guide future neuromorphic device design. Further details on the learning algorithm and its implementation can be found here.[291]

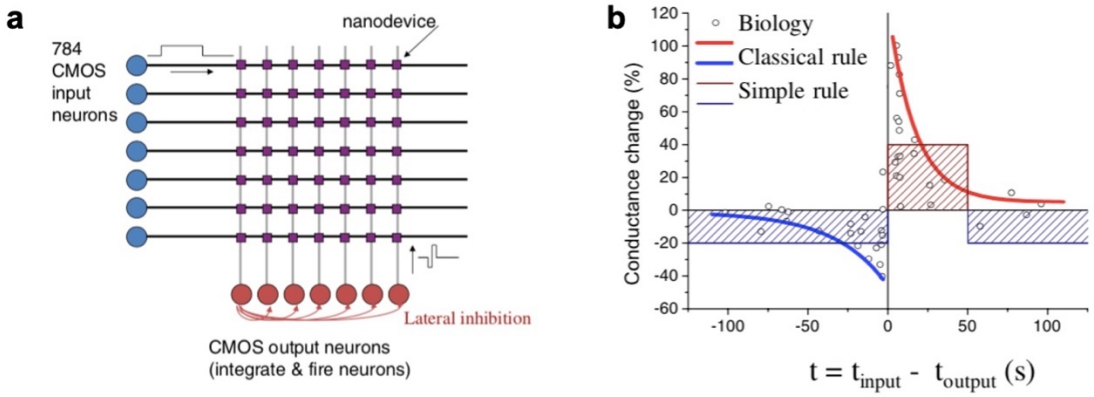

Figure 5.2 | Spiking neural network using STDP. a, Schematic crossbar array architecture for a 2-layer spiking neural network. The first layer is the input layer where the input from a 28 x 28 pixel MNIST image is flattened into 784 input neurons . **b,** Synaptic conductance change as a function of spike-timing (i.e. $t_{input} - t_{output}$) for biological neurons (white circles), classical STDP rule (blue and red lines), and a simplified STDP rule (blue and red dashed boxes). © 2013 IEEE. Reprinted, with permission, from [291].

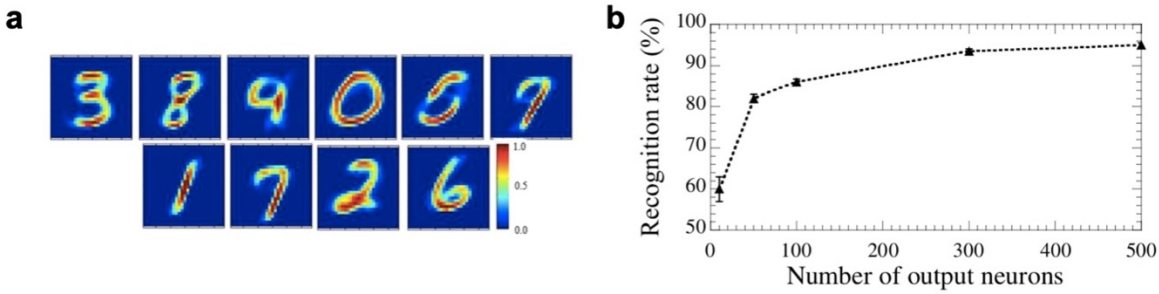

Figure 5.3 | Results of trained spiking neural network. a, 2D bitmaps of synaptic weights, where each image shows how a trained output neuron has learned a hand-written digit from the MNIST data set. Each image corresponds to the 784 synaptic weights of a single output neuron and each colored pixel corresponds to the weight of a synapse. **b,** Recognition rate as a function of the number of output neurons in a network, showing how increased redundancy leads to recognition rates as high as 94%. © 2013 IEEE. Reprinted, with permission, from [291].

5.3 Electrically-driven single-photon emitters

As previously discussed in Section 2.2.2, another emerging high-impact application of SWCNTs is the development of single-photon emitters (SPEs) that support quantum information systems.[18,292] To date, SWCNT-based single-photon emission has only been achieved using optical pumping, limiting their impact in practical optoelectronic systems.[156,159,160,164] Therefore, this section describes a project in progress that would achieve a significant milestone in SWCNT-based optoelectronics: electrically driven, SWCNT-based SPEs.

High purity chiral enrichment of SWCNT dispersions is a pre-requisite for optoelectronic applications since SWCNT optical emission is dependent on chirality. To this end, initial efforts have focused on chiral enrichment of SWCNT dispersions, primarily (6,5) SWCNTs due to the commercial availability of (6,5)-enriched SWCNT powders (Sigma Aldrich SG65i). Figure 5.4 shows the PL map for polymer-wrapped (PFO-BPy) (6,5) SWCNTs dispersed in toluene, where the characteristic E_{11} peak for mobile exciton emission can be seen (~995 nm). While these solutions achieved (6,5) chiral enrichment and could be characterized in solution, the low concentration of SWCNTs (<0.01 mg/mL) made them incompatible with established processing methods for high performance devices. To overcome this limitation, current work focuses on using gel chromatography to achieve solutions with both chiral enrichment and high SWCNT loading.[192]

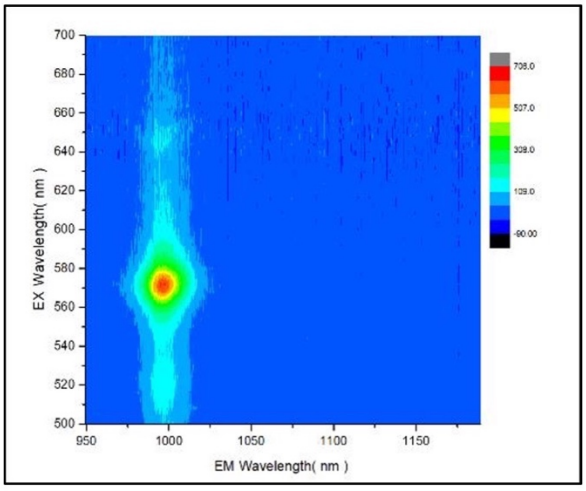

Figure 5.4 | Excitation-emission spectra of polymer-wrapped (6,5) SWCNTs. a, PL maps showing the excitation-emission spectra for (6,5) SWCNTs dispersed with PFO-BPy polymer in toluene.

While conventional emission in SWCNTs results from trapping and recombination of excitons at shallow, localized states, single-photon emission has been achieved primarily through deep states introduced by defects from covalent functionalization.[156,158,159] Therefore, initial work will focus on introducing aryl sp^3 defects via reactions between (6,5) SWCNTs in solution and diazonium salts in deuterium oxide due to their compatibility with SWCNTs dispersed in both aqueous and organic solvents.[293] As shown in Figure 5.5, this covalent functionalization results in red-shifted brighter emission in the near-IR regime, where the change can be tuned through reaction time and concentration of the diazonium salts.[294] Furthermore, the versatility of diazonium chemistry will enable the study of SWCNT emission with a wide range of organic groups, which is of value for tunable emission and optimization.

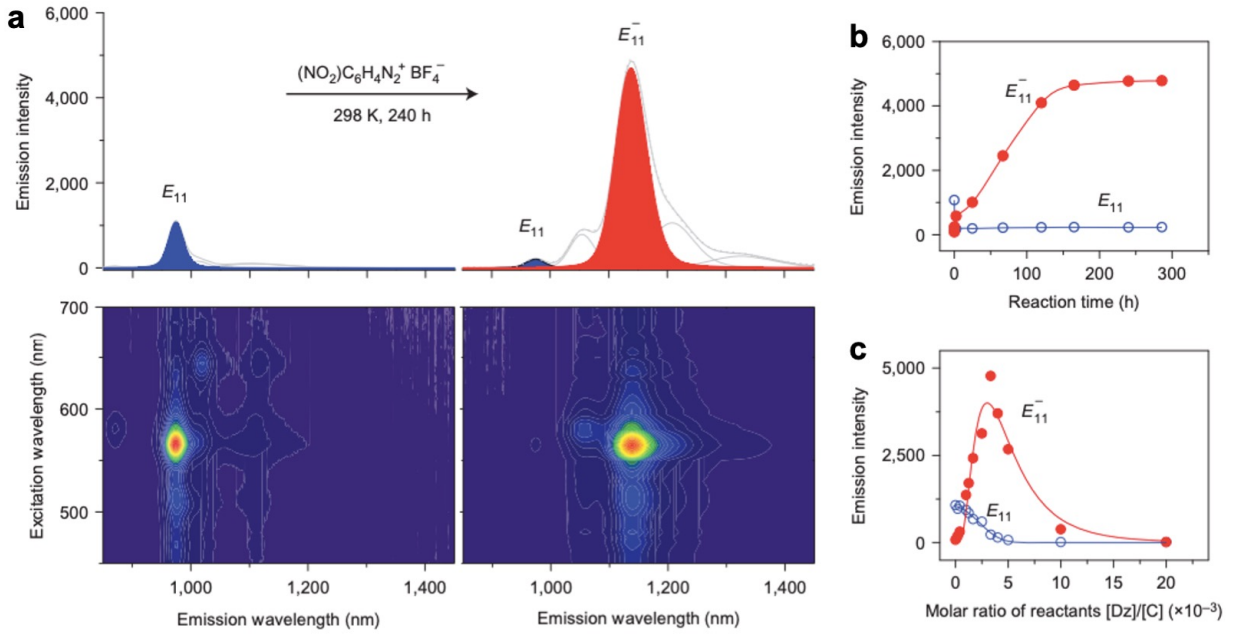

Figure 5.5 | Exciton PL in diazonium-functionalized (6,5) SWCNTs. a, PL spectra (top) and PL map (bottom) of (6,5) SWCNTs before (left) and after (right) functionalization with 4-nitrobenzenediazonium tetrafluoroborate which gives rise to a new red-shifted, brighter peak (E_{11}^-). **b,c,** This emission brightness of the new peak is dependent on reaction time (**b**) and molar ratio of reactants in the diazonium salt (**c**). Reprinted by permission from Springer Nature: Nature Communications,[294] Copyright (2014).

Once both chiral enrichment and optimized covalent functionalization are achieved, we can use processing methods developed in this thesis to fabricate electrically-driven emitters. These electrically-driven emitters will leverage our understanding of processing-property relationships in charge transport devices to expedite investigation and optimization of electroluminescence from SWCNT defect states. With collaboration from local experts in organic functionalization, we hope to further expand the understanding of room temperature, electrically-driven emission, with the aim of achieving electrically-driven single-photon emission.

5.4 General outlook

Two decades of fundamental research has established the potential of SWCNTs in a broad range of computing applications. However, key engineering challenges still need to be overcome before SWCNT-based technologies can reach their full commercial potential.[1,8,10,22,76] From the perspective of SWCNT structural control, further developments in controlled growth and/or post-synthetic purification are needed to achieve SWCNT chirality and enantiomeric enrichment with high purity and high yield. While significant progress has been made towards these goals, the efficacy of many computing applications, particularly those highlighted in Sections 2.2 and 2.3, may be limited by relatively low chirality[40,51,57] and enantiomer[186] purity levels (< 90%) when compared with devices based on electronic-type SWCNTs with ultrahigh purity. Furthermore, monochiral and enantiomer enrichment methods have primarily focused on a limited number of SWCNT chiralities, most notably (6,5) SWCNTs. Therefore, future work focused on monochiral and enantiomerically pure SWCNT structural control should develop schemes that can be generally applied to the full range of SWCNT chiralities.

A parallel challenge is the high-throughput quantification of SWCNT purities well beyond 99%. For the past decade, post-processing purification methods for electronic-type enrichment (i.e., s-SWCNTs) have routinely achieved purity levels beyond the detection limit of currently available optical characterization techniques.[15,41,55,105] Although further purity characterization has been achieved through costly fabrication and electrical characterization of a large number of individual SWCNT FETs,[15,105] this laborious method is prohibitively time and resource intensive

for future applications requiring m-SWCNTs impurities below 1 ppb.[1] Moreover, the absence of a readily available high-throughput characterization method for identified residual impurities in high-purity (> 99%) samples has significantly slowed efforts to further improve s-SWCNT enrichment methods. As the purity achieved in monochiral and enantiomer-enriched samples reach similarly high levels,[34,186] analogous characterization challenges can be expected. Therefore, future research should seek high-throughput characterization methods for quantifying electronic type, chirality, and enantiomeric purities beyond 99% in addition to rapidly identifying the identity and concentration of residual impurities.

While improved monochiral and enantiomeric enrichment methods are likely to impact a broad range of device applications,[3,5,33] these chemically pure samples are particularly important for highly-selective SWCNT-based molecular recognition systems. In particular, monochiral and enantiomerically pure SWCNTs species provide opportunities for improved chemical selectivity especially for high-value biological and pharmaceutical targets that often require enantiomeric differentiation. Similarly, monochiral and enantiomerically pure SWCNTs provide opportunities for separating small molecule enantiomers from racemic mixtures by exploiting enantiomer-dependent adsorption. By diversifying the range of monochiral and enantiomerically pure SWCNTs beyond the canonical (6,5) chirality, tailored sensor arrays can then be generated to enable highly-selective multiplexed molecular sensing.

Assuming that multiplexed SWCNT sensor arrays are realized, then demand will increase for SWCNT mixed-signal ICs that can minimize the need for external Si electronics to amplify and process sensor array outputs. These mixed-signal ICs would ideally be capable of receiving multiple analog inputs, as well as performing signal conditioning, digitization, and processing.

Consequently, these systems will require the development of both analog and digital signal processing functions.[1,4] However, despite the significant amount of research that has been devoted to SWCNT ICs, the vast majority of these studies have focused exclusively on digital applications. Therefore, future work should focus more equitably on the development of analog functions in addition to their integration with existing digital components to achieve seamless mixed-signal operation.

In high-performance digital applications, the aggressive scaling of transistor channel lengths below 5 nm represents a significant challenge. While reduction of both the channel length and transistor footprint in SWCNT FETs at this technology node is predicted to result in considerable improvements in key metrics, most notably the energy-delay product,[1,126] scalable and cost-effective manufacturing methods at the 5 nm scale are not yet established. In particular, significant effort is still required to develop methods for assembling SWCNTs in optimal FET geometries (e.g., aligned arrays with sufficient spacing to minimize tube-tube screening effects) at wafer-scale. An alternative 3D integration scheme to effectively increase device density would be to stack multiple CNT logic layers on the same chip, although this approach will likely require clever heat management and power dissipation schemes, particularly for the interior logic layers that are spatially removed from traditional heat sinks and related convective cooling schemes.

Given the unique advantages of SWCNT optical detectors and emitters,[5,11,171] VLSI system-on-a-chip integration of SWCNT-based optical and electronic components would enable a range of next-generation computing systems. Most directly, the development and integration of high-density optical interconnects with SWCNT-based optoelectronic devices would allow the replacement of on-chip metal lines with high-speed photonic lines for enhanced data transfer rates.

In the longer term, this technology could be further combined with other emerging technologies, such as single photon emission and detection, to realize quantum sensors and computing elements. However, it should be noted that SWCNT single photon detectors are significantly less developed than SWCNT single photon emitters, so this technology gap will need to be addressed before SWCNTs will be viewed as serious contenders among the increasing number of proposed materials and approaches for quantum technologies.

SWCNTs are also promising candidates for hardware accelerators for artificial intelligence, machine learning, and neuromorphic computing. While advances in neuromorphic architectures have already demonstrated energy efficiency advantages for artificial learning paradigms,[137,140] further development of other neuromorphic functions and large-scale integration with SWCNT analog and digital components are still needed. Ultimately, this line or research has the potential to realize 3D monolithic fabrication of comprehensive brain-inspired nanosystems that combine logic, memory, and neuromorphic components. When combined with optimized software, such neuromorphic systems have the potential to overcome performance bottlenecks in artificial neural networks and machine learning applications.[130,137] As highlighted in Figure 5.6, any number of these technologies could be readily integrated on a single chip, facilitating the development of computing components capable of meeting a wide array of mechanical, electronic, and functional needs. Overall, with diverse opportunities in integrated sensing, photonics, quantum information sciences, and beyond-von-Neumann architectures, chirality-enriched carbon nanotubes are among the most promising foundational material platforms for next-generation computing technologies.

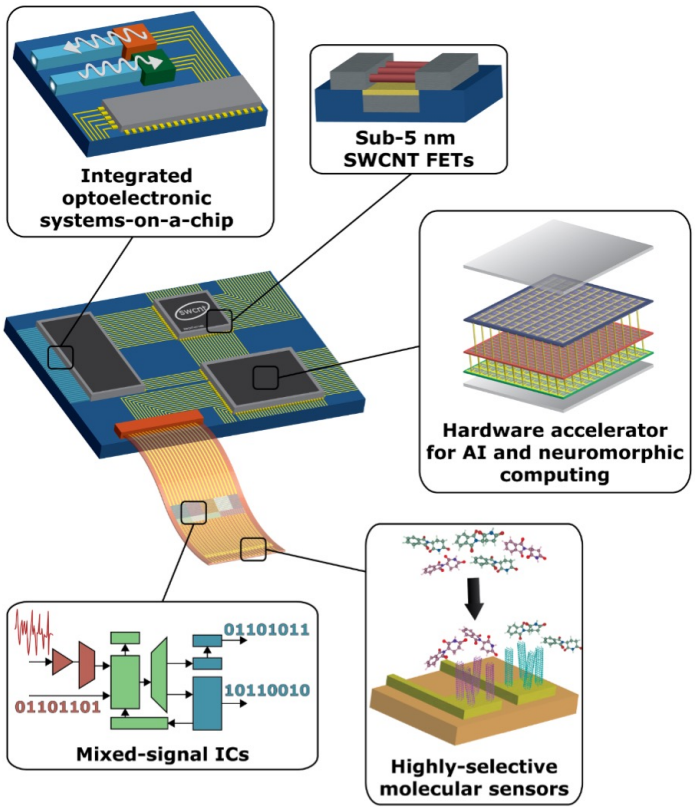

Figure 5.6 | Next-generation SWCNT-based computing system. Diagram of potential next-generation SWCNT-based computational elements integrated into a single system. The SWCNT structures were generated using the TubeGen 3.4 web interface.[19] Reproduced with permission.[20] Copyright 2020, Wiley-VCH Verlag GmbH & Co. KGaA, Weinheim.

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Massachusetts Institute of Technology — **Cambridge, MA**
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Honors

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NSF Graduate Research Fellowship. Awarded to top 12% of applicants (2015)
GEM PhD Engineering Fellowship. Awarded to top 7% of applicants (2015)
IEEE Charles LeGeyt Fortescue Graduate Scholarship. Awarded annually to a single graduate student in EE in the US (2014)
Walter P. Murphy Fellowship – EECS Department at Northwestern University. (2013)
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Research & Industry Experience

Northwestern University – Hersam Research group — **Evanston, IL**
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Publications

1. **W.A. Gaviria Rojas***, et al*. "Solution-processed ohmic-contact-gated transistors for high performance amplifiers" (draft).
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