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Investigation of Carrier Transport in Semiconductor Nanowires by Scanning Probe Techniques

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ABSTRACT

Investigation of Carrier Transport in Semiconductor Nanowires by Scanning Probe Techniques

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In this work, electron beam induced current (EBIC) and scanning photocurrent microscopy (SPCM) were used to quantitatively investigate the electronic properties of silicon nanowire devices. For the first time, it was shown that minority carrier diffusion lengths in phosphorous-doped silicon nanowires are significantly reduced from their bulk values because of nonradiative recombination at the nanowire surface. Diffusion lengths were measured quantitatively by EBIC analysis of nanowire Schottky diodes.

SPCM analysis of two-terminal ohmic n-type silicon nanowire devices revealed a nonuniform electric field along the channel length suggesting an increased resistivity toward the nanowire tip. Etching of the nanowire surface eliminated the gradient indicating that the origin was a surface doping profile. Using four-terminal device geometries, it was shown that quantitative one-dimensional potential profiles and effective carrier concentrations may be obtained. The surface etching process was also used to fabricate high-performance n-Si nanowire FETs that operate based on the n^+-n junctions introduced

by the etch. SPCM confirms that, in the subthreshold regime, the dominant resistance in the device becomes the n^+-n junctions at the edges of the etched region while in the on-state modulation of the carrier concentration in the etched channel determines the device transfer characteristics.

The effect of nanowire nonuniformity on FET performance was investigated using tapered boron-doped silicon nanowires. The transistor threshold voltages and subthreshold slopes were shown to change monotonically along the length of the nanowire with improved transistor characteristics at the tip. SPCM analysis indicated the relative contribution from contact resistance increased toward the nanowire tip where the carrier concentration is reduced in the absence of significant surface doping.

A combination of current-voltage analysis and SPCM was used to investigate silicon nanowire Schottky diodes. Schottky barrier properties obtained by the two methods show good agreement and were used to estimate the internal electric field at the metal-semiconductor junction as well as the effective carrier concentration of the semiconductor.

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as one. You have been more patient than I could have ever asked and reaching this point feels like a dream. Even from a distance your encouragement and support is what helped me succeed and strive to do better. I can only imagine what we will achieve together. I love you.

List of Abbreviations

AFM ..... Atomic force microscopy

CVD ..... Chemical vapor deposition

EBIC ..... Electron beam induced current

EBL ..... Electron beam lithography

FET ..... Field-effect transistor

HRTEM .... High-resolution transmission electron microscopy

KPFM ..... Kelvin probe force microscopy

MOSFET ... Metal-oxide-semiconductor field-effect transistor

PCB ..... Printed circuit board

SEM ..... Scanning electron microscope

SIMS ..... Secondary ion mass spectrometry

SPCM ..... Scanning photocurrent microscopy

STEM ..... Scanning transmission electron microscope

TEM ..... Transmission electron microscope

VLS ..... Vapor-liquid-solid

VS ..... Vapor-solid

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CHAPTER 1

Introduction

The ways in which people receive, process and store information have been revolutionized over the last twenty to thirty years thanks to incredible advances in computing technology. Gordon Moore, co-founder of Intel Corporation, famously predicted that the number of integrated components per chip would double every two years, known as Moore's Law[1]. Since the original (revised) prediction in 1975, this trend has been maintained through a staggering series of scientific advances and engineering triumphs. While, even today, major technology companies continue to push the limits of processing technology, it is the belief of many that traditional top-down fabrication procedures will soon reach their ultimate potential. This has driven those in the research community to pursue radically different approaches based on bottom-up fabrication using self-assembled building blocks[2].

Semiconductor nanowires are an example of this type of building block that, together with carbon nanotubes, have been predicted to give performance gains over traditional devices owing to decreased carrier scattering in quasi one-dimensional conductors[3,4]. While this has not been demonstrated experimentally, there has been significant progress in nanowire-based devices over the last ten years[5] with successful integration into a wide variety of traditional semiconductor devices including transistors[6–9], photodiodes[10], LEDs[11,12], lasers[13,14], and solar cells[15,16]. Furthermore, advances in alignment[17,18] and large-area integration[19] have enabled fabrication of more complicated structures such

as nanowire-based logic circuits[20] and imaging sensors[21]. Other applications have taken advantage of the unique geometry of nanowires (nanowire resonators for mass sensing[19]) and high surface area-to-volume ratio (chemical and biological sensing[22]). Arrays of nanowire devices were even interfaced with living neuron cells to demonstrate the ability to spatially resolve neurological signal propagation and locally stimulate activity[23]. Although progress has come quickly, the near-term promise of nanowire-based technologies varies greatly across the aforementioned applications.

None of these exciting demonstrations have shown great enough advances in performance or function to warrant the billions of dollars in industrial development investments from which traditional semiconductors have benefited. It is futile to target mature industrial markets with decidedly immature materials that, in many cases, lack quantitative metrics and standards for characterization. Optimization of nanowire devices will first require improvements in the structure, composition, uniformity and morphology of the nanowires themselves. Such improvements will require the development of characterization techniques that can provide quantitative information about material properties from which progress can be measured. In many cases, existing practices for materials characterization are not applicable or cannot be scaled sufficiently for use with nanostructured materials like nanowires, thus creating a need for innovation.

In this work, development of new techniques for the analysis of semiconductor nanowires will be presented along with specific advances in the scientific understanding of silicon nanowires. The focus of the study is electrical characterization of silicon nanowire devices because of the technological relevance of silicon as a material and the extensive knowledge-base regarding bulk and thin film properties. Measurements are based on the combination

of current-voltage characterization and scanning probe microscopy. The specific scanning probe methods employed are electron beam induced current (EBIC) and scanning photocurrent microscopy (SPCM), both of which use locally injected charge carriers as a probe of local electric fields. As will be shown herein, scanning probe instrumentation can enable spatially resolved property measurements in integrated nanowire devices with high sensitivity.

Chapter 2 contains background information necessary to explain and contextualize the work in this study, and Chapter 3 covers the experimental setup and procedures for the measurements. In Chapter 4, the application of EBIC to quantitatively determine minority carrier diffusion lengths in n-type silicon nanowires will be presented. A strong diameter dependence of the diffusion length indicates surface dominated transport with surface recombination being the prevailing recombination mechanism. Surface recombination velocity and interface state density are determined quantitatively and are consistent with native oxide on silicon along an unoptimized surface plane. The results are the first quantitative analysis of nanowire devices using EBIC and the first to accurately measure the effects of surface recombination in silicon nanowires.

The issue of doping uniformity will be addressed in Chapter 5. Even in traditional semiconductor technology, at highly scaled dimensions non uniformity in doping can become an issue for device performance. Here, SPCM is used to detect a concentration gradient along the growth axis of phosphorous-doped silicon nanowires. The significance of the result is far-reaching and has implications not only for uniformity of devices along the wire, but also for fundamental limitations in the fabrication of wires with controlled

compositional variations. It is further shown that the gradient arises from a surface doping layer that can be removed by surface etching. A method to extend the quantitative utility of SPCM of nanowire devices is proposed allowing for the accurate determination of one-dimensional potential profiles. Finally a simple model for the measured local photocurrent is used to extract effective carrier concentration profiles before and after surface etching. This provides a quantitative comparison of the nanowire before and after the removal of surface doping.

In Chapter 6, SPCM is used to investigate the principles of operation of a high-performance n-type silicon nanowire field-effect transistor (FET). The sensitivity to local fields provided by SPCM enables a thorough analysis of the device performance as well as facilitates identification of deviations from typical FET behavior. The nanowire FET is fabricated by surface etching of an n-type silicon nanowire. Heavily doped regions at the contacts result in low contact resistance while the reduced doping in the middle of the channel allows for effective modulation of the Fermi level. It is shown that in accumulation current modulation results from enhancement and depletion of electrons in the etched channel while in depletion n^+-n junctions dominate transport. This is in contrast to typical uniformly doped nanowire FETs that operate as Schottky barrier FETs with contact resistances dominating transport in depletion and limiting the device transconductance.

Another issue arising from wire non uniformity is brought to light in Chapter 7 where it is shown that in a p-type silicon nanowire FET, only a small portion of the device channel is effectively modulated by an external field. Common nanowire device analysis methods include many assumptions regarding operation, one of which is a uniform modulation of

the entire device channel. However, SPCM analysis reveals that in a tapered structure with surface doping, the narrow (and therefore less doped) end of the device channel determines the transfer characteristics of the device. This clearly indicates a need to more carefully consider the use of a number of now standard conventions.

Finally, Chapter 8 presents the analysis of n-type silicon nanowire Schottky diodes. SPCM is used to probe the local band bending at the metal-semiconductor interface, and current-voltage characterization is used to extract estimated barrier heights. The built-in potential determined by SPCM and the barrier height extracted using traditional planar models are in close agreement. The barrier parameters are then used to estimate the internal electric fields and doping levels for two different metal-silicon junctions. These results are an important step toward understanding abrupt junctions in nanoscale materials.

CHAPTER 2

Background

The purpose of this study is to correlate chemical and structural information with electronic property measurements and device performance of semiconductor nanowires. The majority of the work focuses on silicon nanowires because of the technological relevance of the material and the extensive knowledge base for silicon properties. This chapter presents the necessary background to motivate, and put into context, the findings of this study.

2.1. Structure and composition of VLS-grown silicon nanowires

Semiconductor nanowires are typically synthesized using chemical vapor deposition (CVD) via the vapor-liquid-solid (VLS) growth mechanism. The growth process, first reported by Wagner and Ellis in 1964[24], involves the use of metal nanoclusters to catalyze one-dimensional crystal growth. The metal particles deposited on an arbitrary substrate are heated to a temperature sufficient to form a eutectic liquid in the presence of a vapor-phase precursor containing the desired semiconductor source atoms. The precursor molecules break down on the surface of the catalyst and form a liquid alloy. With continuing flow of the source material, eventual super-saturation of the droplet leads to crystal nucleation and growth. Growth continues with a constant liquid-solid interface resulting in one-dimensional crystal growth with the catalyst particle remaining at the top of the final structure.

The VLS method of nanowire growth is easily the most common as it offers a number of key advantages. Crystal dimensions can be closely controlled with length being dictated by growth time and diameter determined by the size of the starting metal catalyst[25–28]. Furthermore it has been shown that by changing the gas-phase reactants, *in situ* crystal doping is possible[29,30], and complex axial and radial heterostructures can be synthesized[9,10,29,31,32].

2.1.1. Geometry and crystallinity

VLS-grown silicon nanowires are typically synthesized using gold as the catalyst metal and source gases of either SiH_4 or $SiCl_4$. Wire diameters as small as 2-3 nm have been demonstrated by using size-controlled gold catalyst particles[25,28] and lengths can be arbitrarily controlled by changing the growth time. Recently, it was reported that using Si_2H_6 results in growth rates of up to 31 $\mu m/min$ allowing for growth of millimeter-long nanowires[33].

High-resolution transmission electron microscopy (HRTEM) studies of VLS-grown silicon nanowires verify that wires can be single-crystal[28] over very long length scales[33] and for a wide range of diameters[24,25,28] (see Figure 2.1. After removal from the CVD reactor, it is common to see the formation of an amorphous oxide layer of 1 to 3 nm[28] although it has been shown that growth in the presence of H_2 can passivate the surface and suppress formation of an oxide[25]. Crystallographic orientation varies depending on wire diameter[25] with large diameter wires ($>$ 20 nm) having predominantly $\langle 111 \rangle$ growth direction and wires smaller than 10 nm preferring $\langle 110 \rangle$. $\langle 112 \rangle$ type growth directions are also observed for intermediate and large nanowire diameters.

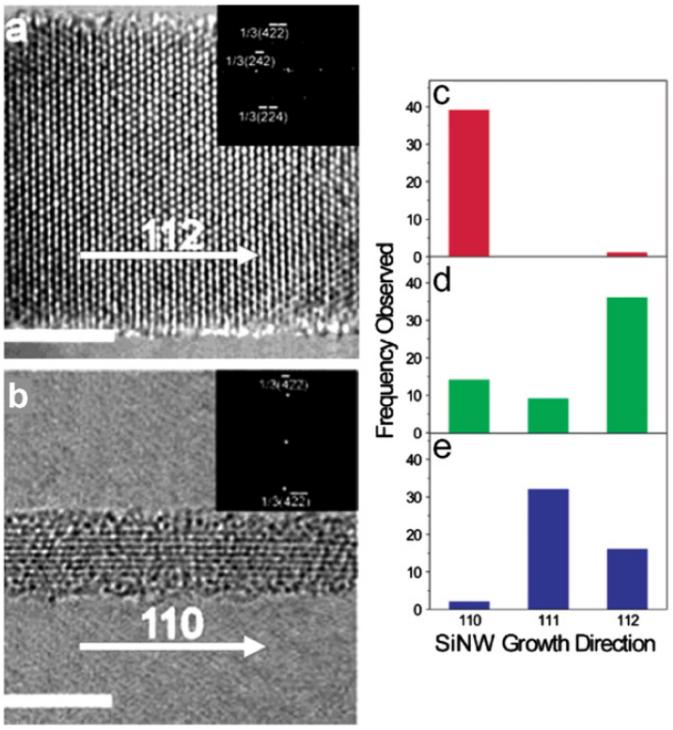

Figure 2.1. Silicon nanowire cystallinity and growth direction. (a) and (b) HRTEM images of silicon nanowire with diameters of 12.3 nm and 3.5 nm respectively. Wires are single crystal. Scale bars are 5 nm. (c)-(e) Histogram of the growth directions for silicon nanowires with diameters from 3 to 10 nm (c), from 10 to 20 nm (d) and from 20 to 30 nm (e). Taken from Lu and Lieber[5].

One-dimensional growth occurs because of enhanced decomposition of source precursor molecules at the eutectic liquid surface combined with selective incorporation at the liquid-solid interface. However, there is also the possibility of two-dimensional vapor-solid (VS) growth if source molecules break down in the vapor phase and elemental species deposit uniformly. This type of concurrent thin film growth results in tapered nanowires as the sides of the wire are exposed to the vapor phase reactants during growth, resulting in greater overgrowth at the base. VS deposition can be promoted by increasing

growth temperatures[34] such that vapor-phase deposition of the precursor molecule happens readily. Furthermore it has been reported that B_2H_6, a common source gas for boron doping in silicon nanowires, can assist in SiH_4 decomposition resulting in increased VS growth[35]. Tapered structures are inherently undesirable for device integration because of the geometrical non uniformity, but there are additional challenges to nanowire devices introduced with VS deposition.

Axial modulation of nanowire composition with changes in either the semiconductor material or dopant atoms presents an intriguing route to synthesis of functional materials at scales below the limits of traditional lithography. However, VS deposition may degrade the quality of axial junctions. Axial homojunctions have been demonstrated in silicon nanowires using phosphorous and boron as dopants for n and p-type segments, respectively[10,29,31,36]. For such structures it is necessary to prevent VS deposition which would result in deleterious overcoating that would obscure the doping modulation. The use of H_2 to passivate the wire surface was mentioned above and can also assist in preventing VS deposition. Furthermore, local substrate heating in place of the more common tube furnace heating can reduce gas-phase decomposition of the source molecules[31]. In the literature, the success of such measures is typically measured using HR-TEM to observe changes in diameter along the nanowire length where it has been found that variation in diameter can be as low as ~1%. A number of reports have shown electrical measurements consistant with axial dopant modulation[29,31], however results are qualitative and cannot rule out some contribution from surface doping. Recently, complex tandem axial p-i-n nanowire photovoltaic devices were demostrated showing multiple high quality axial junctions[36] that were identified through selective surface etching 2.2; however wires used

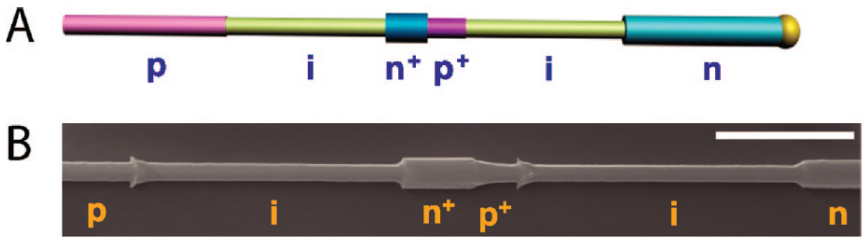

Figure 2.2. Axial modulation doping in a silicon nanowire. (a) Schematic of a functional modulation-doped nanowire structure consisting of two p-i-n diodes in series. (b) SEM image after selective etching of an axially modulated p-i-n^+−p^+-i-n silicon nanowire. Scale bar is 1 μm. Taken from Kempa et al.[36]

in this study were subjected to dry oxidation and etching following synthesis in order to remove a surface coating that the authors point out may lead to current leakage in their axial junctions.

2.1.2. Compositional analysis of dopants and other impurities

While it has been clearly demonstrated that doping of silicon nanowires is possible, determination of the dopant concentration is challenging. Typical silicon doping levels for device applications can range from 1×10^{13} cm^{-3} to 1×10^{20} cm^{-3} corresponding to a maximum atomic impurity concentration of 0.2%[37]. Therefore detecting dopant atoms in silicon nanowires requires extremely high sensitivity.

Secondary ion mass spectrometry (SIMS) is a common method for determining the chemical composition of semiconductors capable of detection limits below one part per billion. Because of the insufficient lateral resolution of traditional SIMS, measurements of nanowire composition have been conducted as an ensemble using the growth substrate[38,39]. Figure 2.3 shows SIMS results for phosphorous and boron doping in silicon nanowires. It

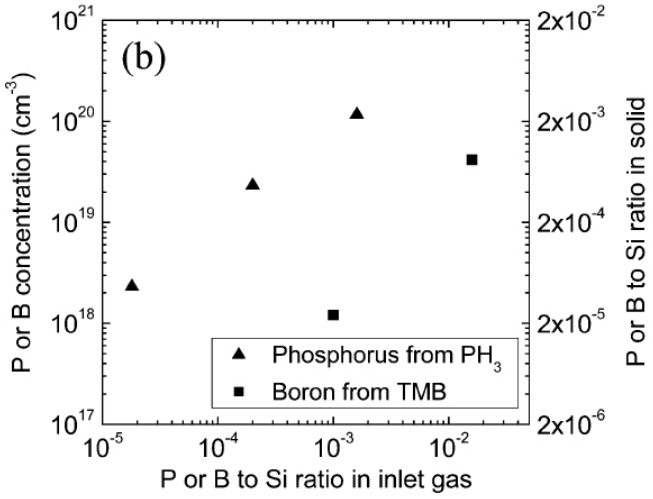

Figure 2.3. Phosphorus and boron concentration in silicon nanowires obtained by SIMS as a function of the dopant-to-silicon ration in the gas phase. Taken from Wang et al.[38]

was shown that both dopant types scale as expected with increased vapor-phase reactant ration. However, the lower detection limit in these measurements was found to be above 1×10^{17} cm^{-3} which was attributed to increased background levels because of the high surface area of the nanowire samples[38]. More recently, local electrode atom probe (LEAP) tomography has been used to investigate the concentration of phosphorous in VLS-grown germanium nanowires[40,41] as well as unintentional impurities such as oxygen[40] and gold[42].

Unintentional dopants may be equally important to the properties of VLS-grown silicon nanowires. The use of gold as a catalyst is particularly hazardous as incorporated gold atoms may compensate majority carriers and act as recombination centers thus reducing carrier lifetimes[43,44]. These effects are shown quantitatively by the plots in Figure 2.4. Recently, in Allen and Hemesath et al.[42], scanning transmission electron microscopy (STEM) was used to confirm the presence of gold impurities in VLS-grown silicon nanowires. Focal series imaging was used to distinguish between surface and bulk

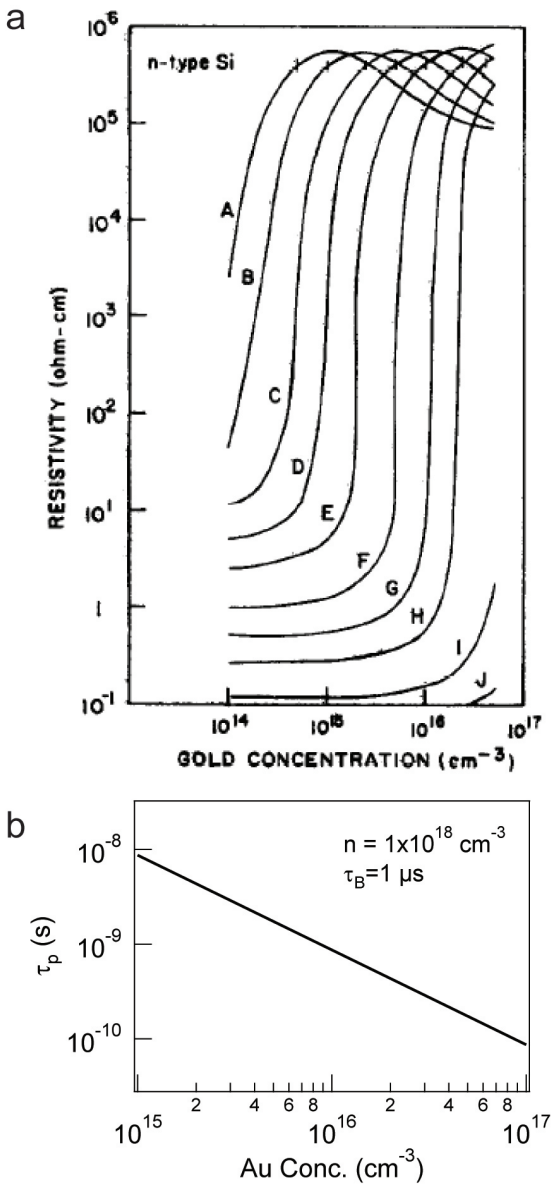

Figure 2.4. Effects of Au contamination in Si. (a) Calculated resistivity vs. gold concentration for n-type silicon at 300 K. A-J are calculated with increasing phosphorus concentrations (cm^{-3}) from 1×10^{14} cm^{-3} to 1×10^{17} cm^{-3}. Taken from Bullis[43]. (b) Calculated minority carrier lifetime vs. gold concentration for n-type silicon at 300 K. Expression for the calculation was taken from Fairfield and Gokhale[44].

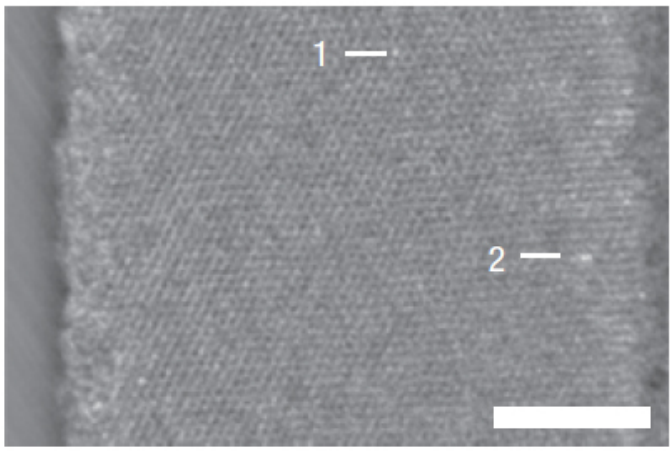

Figure 2.5. Abberation-corrected STEM image of gold atoms in a VLS-grown silicon nanowire. Scale bar is 5 nm. Taken from Allen and Hemesath et al.[42]

gold atoms, and it was found that incorporation was above the equilibrium concentration at the nanowire growth temperature. The presence of gold contamination in silicon nanowires was further confirmed by another STEM study reported at around the same time[45]. Nano-SIMS measurements of gold concentration levels in large diameter (1-2 μm) silicon nanowires grown with $SiCl_4$ provide an upper-bound of ~1.7×10^{16} cm^{-3}. This is approximately equal to the equilibrium concentration for the growth temperature of 1000 °C in this case. The importance of gold contamination cannot be overlooked; however, commonly used nanowire doping levels are significantly higher than the gold concentration and recombination is dominated by surface recombination as will be shown in Chapter 4.

2.2. Electronic properties of silicon nanowires

There are still many challenges in accurately determining electrical properties of nanoscale materials. In bulk and thin film materials, majority carrier concentration and

mobility can be determined using well-established techniques such as Hall effect measurements. Furthermore, minority carrier mobility can be measured using the Haynes-Shockley time-of-flight method. However, for both of these standard techniques, application to nanowires is not straight forward and have not yet been demonstrated. Instead, the vast majority of work on nanowires has focused on device property measurements rather than fundamental property measurements. This section will focus on reported methods for extraction of electronic properties of silicon nanowires including carrier concentration, mobility, and interface state density.

2.2.1. Carrier concentration and mobility

In section 2.1.2, SIMS analysis of the dopant concentration of silicon nanowires was presented showing that dopant incorporation increases with increasing gas phase ratio. Figure 2.6 shows a plot of nanowire resistivity versus gas phase ratio clearly indicating that the resistivity decreases with increased dopant-to-SiH_4 ratio[46]. Correlating this data with the SIMS data indicates that some fraction of the incorporated dopants are electrically active. Resistivity values for nanowires are typically obtained using four-probe devices which allow for an accurate determination of the total wire resistance. Details of this technique are presented in Chapter 3. With the total wire resistance known, the average resistivity is calculated based on geometrical factors determined using a scanning electron microscope (SEM) or atomic force microscope (AFM). For the four-probe analysis, it is assumed that conduction occurs uniformly across the nanowire cross-section and that current flow is confined to the wire rather than possible parallel conduction paths through the

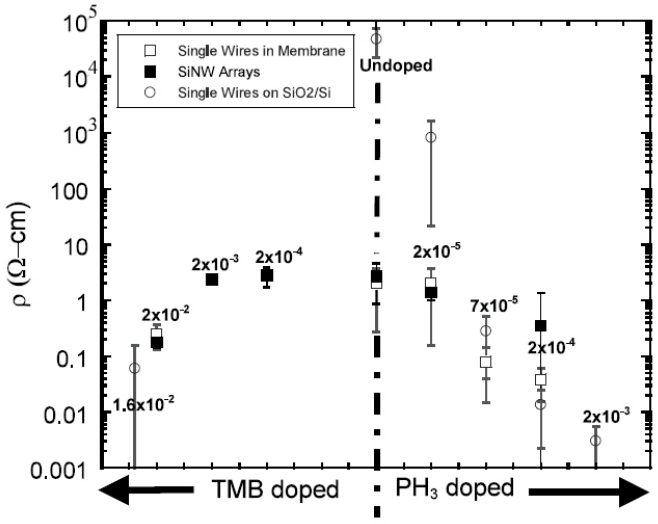

Figure 2.6. Plot of resistivity versus dopant-to-SiH_4 ratio for both phosphorous and boron doping. Taken from Eichfeld et al.[46]

inner electrodes. Despite these assumptions, it is still one of the most reliable nanowire property measurements to date.

Using a measured resistivity, it is common to approximate the carrier concentration using the relationship, $n = 1/\rho e\mu_n$, and a bulk value for the mobility[47–49]. Applying this relationship to the range of resistivity values plotted in Figure 2.6 yields a range of carrier concentrations from ~1×10^{16} cm^{-3} to 2×10^{19} cm^{-3}. It has been reported that undoped silicon nanowires grown using VLS are unintentionally doped p-type and show resistivities of 3.9×10^{2} Ω cm[30] corresponding to a doping level of almost 1×10^{14} cm^{-3}.

Mobilities in nanowires may vary significantly from their bulk counterparts due to increased scattering at surfaces and unintentional impurities. It has also been suggested that at small diameters, nanowires and other quasi-one-dimensional materials, such as carbon nanotubes, may exhibit enhanced mobilities with decreased scattering due to quantum confinement effects[3,4]. Therefore, mobility measurements on nanowires are desirable

to quantify these differences and improve the accuracy of estimated carrier concentrations. Typically, mobilities of single VLS-grown nanowires are estimated based on the transfer characteristics of nanowire field-effect transistors using an estimated gate capacitance[6,7,32,50–53]. The method for determination of the field-effect mobility is detailed in Chapter 3. While this method is widely applied, it is often acknowledged that this is a device parameter and could potentially deviate significantly from the true mobility. For example, it was shown in Zheng et al.[53] that for n-type silicon nanowire FETs the field-effect mobility was actually higher for more heavily doped wires. This was attributed to the increased contribution from contact resistance at lower doping levels limiting the observed transconductance. Furthermore, the field-effect mobility requires an estimation of the gate oxide capacitance which is typically too small to measure directly. To date, there have been two reports of gate capacitance measurements in nanowires devices. Gunawan et al.[54] presented the direct measurement of gate capacitance in lithographically defined silicon nanowire devices. Approximately 1000 devices were measured in parallel increasing the total gate capacitance to a measurable quantity. The resulting value is therefore an average, and the technique cannot be applied to individual VLS-grown nanowires. In the next example, Tu et al.[55] used a capacitance bridge capable of measurements down to 30 aF to directly measure the gate capacitance of a germanium nanowire FET. Capacitances were on the order of ~1 fF and were supported with simulated values for various device geometries. This is an impressive measurement, however device performance measurements are necessary to extract a carrier mobility. Quantitative capacitance measurements are an important step in the understanding of nanowire devices, however this alone cannot give an accurate mobility measurement.

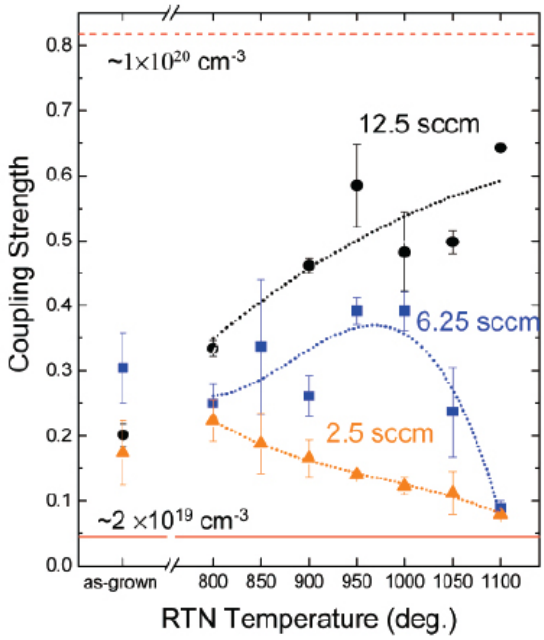

Figure 2.7. Fano resonance coupling strength versus annealing temperature for p-type silicon nanowires with different B_2H_6 gas flow rates; 2.5 sccm (triangles), 6.25 sccm(squares), and 12.5 sccm (circles). The solid and dashed horizontal lines represent the coupling strength values obtained for boron-doped silicon wafers with doping levels of 2×10^{19} and 1×10^{20} cm^{-3}, respectively. Taken from Eichfeld et al.[56]

Recently it was demonstrated that carrier concentration can be determined in heavily boron-doped silicon nanowires using Raman spectroscopy[56,57]. In heavily doped p-type silicon, Fano resonance arises due interference between discrete phonon Raman scattering and continuous electric Raman scattering from intraband hole transitions. The result is an asymmetry in the Raman peak which can be used to quantify the carrier concentration. Figure 2.7 shows a plot of the Fano resonance figure of merit, the coupling strength, versus annealing temperature for wires grown with varying B_2H_6 flow rates. The as-grown wires show carrier concentrations between 2×10^{19} and 1×10^{20} cm^{-3}; however within that range only relative carrier concentrations are discussed. Also indicated by this plot is that

not all of the incorporated dopants are electrically active in as-grown wires. Following annealing steps the coupling strength increases as more dopants are activated and the carrier concentration increases.

2.2.2. Interface state density and surface recombination

At highly scaled dimensions, the influence of the surface on electrical properties becomes increasingly important. It is known that even in commercial metal-oxide-semiconductor field-effect transistors (MOSFETs), it is necessary to control the surface oxide to minimize surface charges that can screen externally applied electric fields and degrade device performance. Interface states which are formed because of incomplete passivation of dangling bonds at the semiconductor surface are a significant contribution to surface charge. Furthermore, high densities of interface states will lead to an increased depletion region near the surface that, at small diameters, could fully deplete the nanowire. Passivation of the interface states in planar silicon is necessary to keep surface charge at a minimum and improve device performance. A number of recent studies have reported values for surface state densities in silicon nanowires.

By examining nanowire resistance versus cross-sectional area, Seo et al. found that boron-doped silicon nanowires become resistive more quickly than the expected A^{-1} dependence for a uniform cylinder. This was attributed to the existence of a depletion region due to positive surface charges which reduce the effective conducting area of the nanowire, A_{eff} (see Figure 2.8). Therefore, one would expect the resistance to vary as ${A_{eff}}^{-1}$ with

$$\mathrm{A_{eff}} = \mathrm{A_{measured}} \left(1 - \frac{2}{\mathrm{r_0}} \frac{\mathrm{N_s}}{\mathrm{N_a}} \right)$$

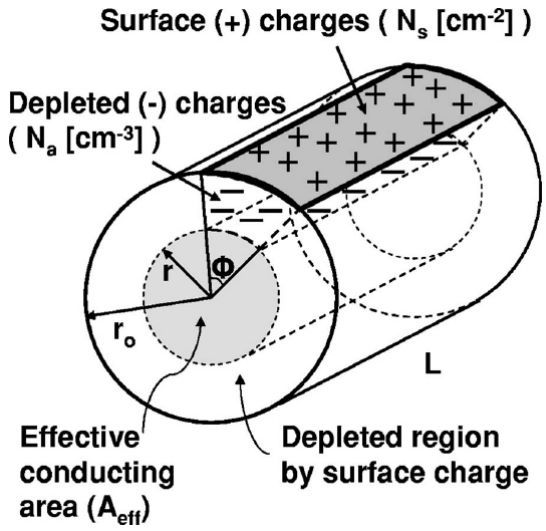

Figure 2.8. Schematic showing depletion near the nanowire surface caused by surface charge. Taken from Seo et al.[49]

where N_s is the interface state density and N_a is the dopant concentration. Fitting the resistance versus cross-sectional area data with $R = \rho(L/A_{eff})$ then gives the resistivity, ρ, and the ratio of surface-charge density to dopant concentration (N_s/N_a). Assuming a uniform resistivity, bulk mobility, and full dopant ionization the dopant concentration can be estimated from the resistivity allowing for an estimation of the surface-charge density. By this method a surface-charge density of 2.3×10^{12} cm^{-2} was determined for nanowires with a native oxide. The authors also presented data for wires with an intentionally grown oxide (dry O_2 at 850 °C for 1.5 min) where it was found that the calculated surface-charge density decreased by an order of magnitude. The decrease in surface-charge density is determined based on an apparent increase in A_{eff} because of increased wire conductivity after oxidation. However it should be noted that at the oxidation temperature there could be significant dopant activation (see Figure 2.7) which complicates the analysis. Furthermore this analysis requires that the dopant concentration is uniform throughout

the wire; however this is not necessarily the case[36,47] (see Chapter 5 for additional information regarding surface doping in silicon nanowires). A similar approach was recently demonstrated by Kimukin et al.[58] in which the nanowire surface was slowly etched and a nonlinear increase in resistance was observed. In this case the surface-charge density for phosphorous-doped silicon nanowires was determined to be 2.6×10^{12} cm^{-2}. As in the previous case, bulk mobility and uniform resistivity were assumed.

A surface state density of 3.7×10^{12} cm^{-2}eV^{-1} was reported by Liu et al.[59] for unintentionally doped p-type silicon nanowires. Wires were oxidized at 900 °C by dry oxidation in the presence of trichloroethane. The introduction of chlorinated gas during oxidation has been shown to reduce interface trap densities in planar silicon devices. In this case the interface state density was calculated based on the subthreshold slope, S, of top-gated nanowire FETs which is theoretically related to the interface state density by[60]

$$\mathrm{S} \approx \frac{\mathrm{kT}}{\mathrm{q}} \ln 10 \left(1 + \frac{\mathrm{C_{it}}}{\mathrm{C_{ox}}}\right) \approx 60 \left(1 + \frac{\mathrm{qD_{it}}}{\mathrm{C_{ox}}}\right) \mathrm{mV/decade}$$

This expression accounts for the parasitic capacitance introduced by a surface depletion layer which can act to reduce subthreshold characteristics. The oxide capacitance, C_{ox}, was calculated based on the thickness of the thermally grown oxide.

The reported interface state densities in these studies all fall within a similar range and are significantly higher than an optimized planar SiO_2-Si interface[61] which can have interface state densities as low as 5×10^{10} cm^{-2}. It is postulated that high interface state densities in silicon nanowires arise because of the non planar bounding surfaces. Surface state densities for planar interfaces are strongly dependent on crystal orientation and surface quality. The cylindrical shape of nanowires necessarily introduces multiple

surface orientations, but also it has been suggested that high curvature can lead to a degraded interface quality[49].

With such high interface state densities, surface recombination could play an important role in nanowire transport. Surface recombination velocity is a measure of the rate of carrier recombination at the surface of a semiconductor and is directly proportional to the interface state density. Therefore, for silicon nanowires where diameters are significantly smaller than the bulk carrier diffusion length it is possible that carrier recombination could be dominated by surface recombination. This will be addressed directly in Chapter 4.

2.3. Scanning probe measurements of semiconductor nanowire devices

In many cases, quantitative characterization of electronic properties is nontrivial for nanoscale materials. In order to optimize semiconductor nanowires and improve device performance, new or adapted methods for parameter determination must be developed. Analysis using scanning probe microscopy (SPM) could potentially offer quantitative information with high sensitivity and spatial resolution. Existing applications of these techniques are mostly qualitative in nature. However, with accurate modeling it should be possible to obtain quantitative information about a wide range of material properties. This section is a review of recent developments in the use of SPM to probe nanowire devices and gain information about local electronic properties.

Typically SPM refers to techniques that use physical probes that scan a sample of interest to form an image of the surface. The images comprise a wide range of types of information including topography, electrostatic potential, and magnetic polarization.

Specifically, studies on semiconductor nanowires using scanned gate microscopy (SGM) will be discussed. SGM uses a biased probe tip to locally perturb a device while device current is recorded as a function of the probe position. Additionally, this section will discuss uses of scanning probe techniques that do not use a physical probe, but rather locally excited excess carriers to retrieve spatially resolved information about a specimen. These include scanning photocurrent microscopy (SPCM) in which a focused laser spot is used to locally excite excess carriers while device current is recorded as a function of beam position, and an analogous technique, electron beam induced current (EBIC), where the excitation source is a focused electron beam.

2.3.1. Identification of compositional variation

There have been a number of studies reporting the use of SPM to locate heterojunctions and homojunctions in semiconductor nanowires. Yang et al. demonstrated the application of SGM to confirm doping modulation in phosphorous-doped silicon nanowires. In this study, modulation-doped n^+-n-n^+ silicon nanowires were synthesized using VLS and integrated into two-terminal devices. SGM results, shown in Figure 2.9, confirm the expected doping profile. A biased AFM tip was used to locally enhance or deplete carriers in the device while changes in current were measured as a function of the probe position. The images confirm that current modulation is far more efficient in the lightly-doped region. When the external field is applied to the degenerately doped n^+ regions, there is little change in conductance as the field is insufficient to deplete these sections, therefore the dominant resistance is still the lightly doped middle region. Upon local gating of the lightly-doped region, the conductance change is observed in the device current giving

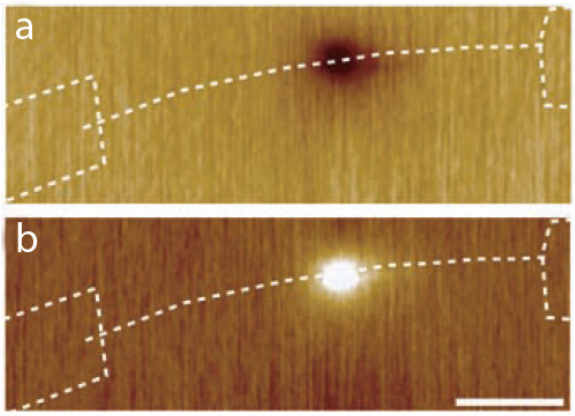

Figure 2.9. SGM images of an n^+-n-n^+ modulation-doped nanowire. (a) and (b) were recorded with a tip bias of -9 V and +9 V, respectively. Source-drain bias was 1 V. The dark and bright regions correspond to reduced and enhanced conductance, respectively. The white dashed lines highlight the positions of the nanowire and electrodes. Scale bar is 1 μm. Taken from Yang et al.[31]

contrast in the image. It was shown that the extent of the contrast in Figure 2.9 matches closely with the expected segment length during synthesis. This is a useful technique for establishing the location and extent of modulation-doped segments which would otherwise be difficult to confirm.

SPCM has also been demonstrated as a technique to locate modulation-doped segments in silicon nanowires[10?] . Changes in device current arise when excess carriers are injected into the device in a region where there is an electric field. Therefore SPCM can be used to map the location of electric fields within a device. Single nanowire avalanche photodetectors were fabricated using modulation doped p-i-n silicon nanowires. As in the previous example, the location and extent of the intrinsic region was confirmed using SGM. Subsequently, a local photocurrent map was obtained using SPCM that shows the active region of the photodetector (see Figure 2.10). The intrinsic portion of the wire

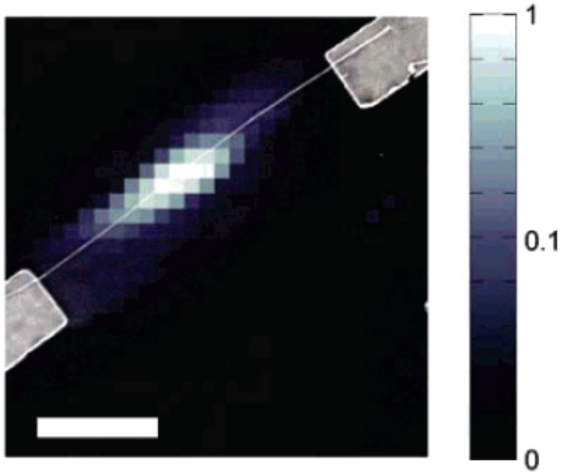

Figure 2.10. Normalized photocurrent map of a p-i-n silicon nanowire avalanche photodiode. Bright contrast corresponds to an increase in device current. Bias voltage was -28 V. Scale bar is 2 μm. Taken from Yang et al.[10]

is the dominant resistance in the device, and therefore one would expect that, under an applied bias, the electric field will be largest in this segment. This is confirmed by the photocurrent map which shows that the largest photocurrent is observed when the intrinsic portion of the wire is illuminated.

Gustafsson et al. recently demonstrated the use of EBIC to locate heterojunctions in InAs-InP heterostructure nanowires[62]. Like the SPCM measurement, EBIC can be used to identify the location of internal electric fields. Figure 2.11 shows EBIC results from an InAs nanowire device with two 12 nm InP tunnel barriers surrounding a 12 nm InAs quantum dot in the middle of the channel. In this case the band bending at the InAs-InP interface gives rise to an internal field. The back-to-back junctions create fields in opposite directions such that the EBIC signal is positive on one side of the junctions and

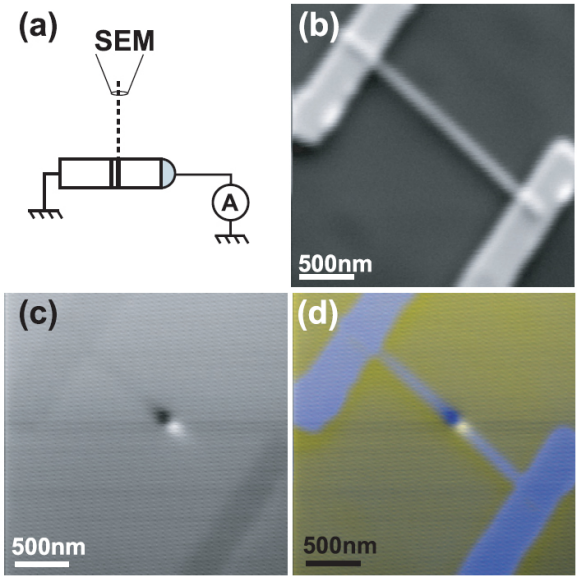

Figure 2.11. Location of nanowire heterojunctions using EBIC. (a) Schematic of the EBIC measurement. (b) SEM image of an InAs nanowire device with two 12 nm InP barriers separated by a 12 nm InAs region in the center of the channel. (c) EBIC map of the device in 'b'. (d) Composite image of 'b' and 'c' showing the location of the EBIC signal. Between the bright and dark contrast is the location of the InAs quantum dot. Taken from Gustafsson et al.[62]

negative on the other. In this report the location of the contrast was used to accurately align top-gate electrodes on top of the isolated InAs quantum dot.

2.3.2. Observation of contact effects

The photocurrent maps provided by SPCM can be used to identify the location of electric fields. Therefore, in devices where contact resistance dominates device transport, large signals are observed at the contacts[63–67]. Figure 2.12 shows SPCM results for a silicon nanowire device with resistive contacts. From the photocurrent line profiles it is seen that at 0 V applied bias there is an equal but opposite photocurrent peak at the two metal contacts. This arises due to the opposing built-in electric fields at the two Schottky

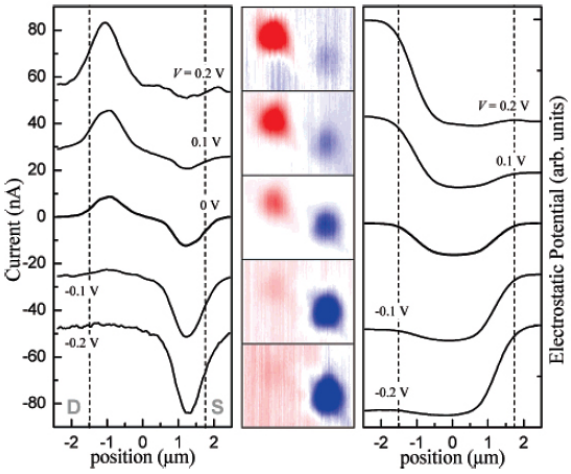

Figure 2.12. Bias dependence of SPCM signal in a silicon nanowire device with two resistive contacts. (Middle column) Color-scale scanning photocurrent images ($3 \times 4\ \mu m$) for different bias voltages. Red (blue) corresponds to an increase (decrease) in current. (Left column) Photocurrent line profiles taken along the nanowire axis. Plots are offset for clarity and dashed lines mark the location of the metal contacts. (Right column) Integrated profiles of the data in the left column (offset for clarity). Taken from Ahn et al.[66]

barriers. Upon applying a bias, the signal at one contact dominates while the other shows little to no photocurrent. This is because one junction will be under a reverse bias while the other is forward biased. Therefore one would expect a much larger electric field at the reverse biased junction and a corresponding photocurrent peak. When the polarity of the applied bias is reversed, the peak shifts to the other contact as this is now the reverse biased junction. The local electric field in the device, $E(x)$, is related to the local potential gradient by $E(x) = -dV(x)/dx$. In the existing literature, it is assumed that the local photocurrent is directly proportional to the local electric field. Therefore, the signal may be integrated to give the device potential profile as shown in the right column of Figure 2.12. This representation of the data reveals the potential drop at the reverse

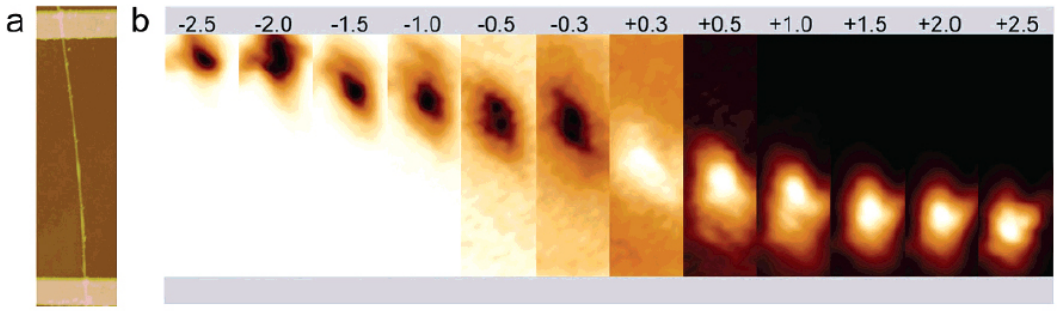

Figure 2.13. SPCM imaging of a CdS nanowire device with two ohmic contacts. (a) AFM topographic image of the CdS nanowire device. Device channel length is 11 μm (b) Sequence of SPCM images with the top electrode biased as indicated. Taken from Gu et al.[68]

biased junction the bias dependence of the potential profile is revealed. However, the interpretation of the SPCM signal in this case is oversimplified as will be addressed in Chapter 5.

2.3.3. Quantitative determination of electronic properties

The above examples of SPM measurements of nanowire devices show useful qualitative information that can be gained by such techniques. However, to optimize the performance of nanowire devices, it is important to develop methods to measure quantitative material properties. Gu et al. recently reported the quantitative determination of electron and hole diffusion lengths in undoped CdS nanowires using SPCM[68]. CdS nanowire devices were fabricated with two ohmic contacts and SPCM measurements were made at different applied biases. It was found that the photocurrent response shows a peak within the device channel that moves monotonically with the applied bias as shown in Figure 2.13.

In this case, the measurement was done in the high-injection regime meaning that the injected carrier density was larger than the equilibrium carrier density. In the applied

electric field, these carriers are separated and some will make it to the contacts before recombining. From the continuity equations, the electron current density at the positive electrode must be equal to the hole current density at the negative electrode. Therefore, a maximum in the photocurrent will exist at the point where the number of excess holes reaching the negative electrode is equal to the number of excess electrons reaching the positive electrode. Moving the excitation away from the positive electrode will reduce the number of collected electrons, thus making electron collection the limiting factor in the photocurrent. In this case the decay of the photocurrent signal will be proportional to the excess electron distribution in the nanowire. Likewise, moving the excitation away from the negative electrode will reduce the hole collection and the decay will be proportional to the excess hole distribution.

Using this explanation for signal decay, it can be said that the decay toward the positive electrode will be related to the average hole drift/diffusion length and the decay toward the negative electrode will be related to the electron drift/diffusion length. Figure 2.14 shows line profiles of the SPCM signal along the CdS nanowire at different applied bias. On a semi-logarithmic scale, an exponential decay of the photocurrent signal is observed on either side of the peak with two distinct decay constants. The line profiles show that the slope of the decay does not change at different applied bias suggesting that the transport of excess carriers in these regions is diffusive in nature. Therefore the extracted decay constants are equal to the carrier diffusion lengths which were found to be ~1.47 μm for electrons and ~0.65 μm for holes.

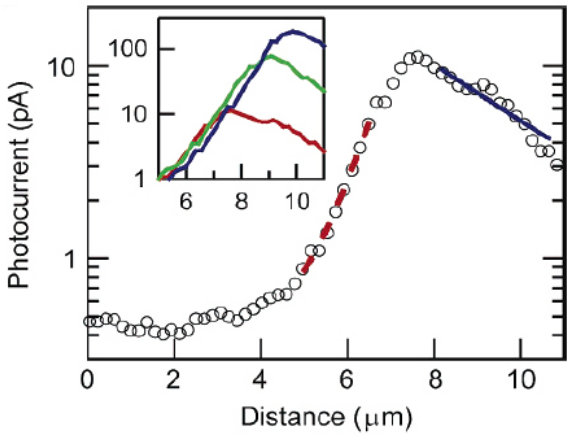

Figure 2.14. SPCM line profiles of a CdS device. Main image is a semi-logarithmic plot of the photocurrent profile taken at 1 V applied bias. The dashed and solid lines are exponential fits to the data. The inset shows line profiles taken at different biases. The slope of the signal decay does not change significantly between scans. Taken from Gu et al.[68]

2.4. Design considerations for nanowire FETs

Since a sudden surge in interest in semiconductor nanowires almost 10 years ago, a wide variety of device applications have been demonstrated. However, much of the initial motivation driving work on nanowires was derived from the promise of high-performance transistors. Silicon is of particular interest for such applications because it is compatible with established processing techniques and is very well studied. Nanowire FETs have been fabricated using uniformly doped p-type and n-type silicon nanowires[6,53] and show device performance comparable to traditional MOSFETs (provided device performance figures of merit are scaled to comparable dimensions[6]). These nanowire FETs are two-terminal devices in which the substrate is used as a back-gate. When an external field is applied using the back-gate, the carrier concentration in the nanowire channel changes modulating the measured device current. However, it has been shown that heavily doped nanowires

show poor transistor behavior while lightly doped nanowires have performance limitations because of high contact resistance[53]. Modulation-doped structures similar to those used in traditional MOSFET devices have been demonstrated but have additional requirements for alignment and fabrication[51,52]. Zheng et al.[53] reported that back-gated nanowire FETs fabricated from heavily-doped n-Si nanowires show better transconductance than lightly-doped nanowires. This is counterintuitive as lower-doped wires should have higher mobility and therefore enhanced transconductace behavior. However, measurements of the contact resistance revealed that high contact resistance in lightly-doped nanowire device may limit the observed transconductance despite an increased carrier mobility. The measured conductance, g_{ex} can be related to the intrinsic conductance, g_{in} by the following relationship:

$$\mathrm{g_{ex}} = \frac{\mathrm{g_{in}}}{1 + \mathrm{g_{in}R_s} + (\mathrm{R_s} + \mathrm{R_d})/\mathrm{R_{wire}}}$$

where R_s and R_d and the contact resistances of the source and drain, respectively, and R_{wire} is the resistance of the nanowire channel[53]. The intrinsic conductance is observed in the limit of zero contact resistance. It was found that the corrected transconductance values scale as expected for decreasing doping levels. While this additional analysis is scientifically useful, it does not change the inherent limitations of the devices. Recently, high-performance Ge/Si core/shell nanowire heterostructures have been used to fabricate nanowire FETs that outperform state-of-the-art metal-oxide-semiconductor FET (MOSFET) technology in most respects[9], but they also exhibit fairly high off-state currents and ambipolar transport unless asymmetric gate geometries are utilized.

In commercial MOSFET devices, the source and drain regions are heavily doped leaving a lightly doped channel region that can be modified with an applied gate bias. To

improve nanowire FET performance, top-gated nanowire devices with similar doping profiles have been fabricated using *in situ* modulation doping[51] and ion implantation[52]. In both of these structures, performance was greatly improved over uniformly doped devices. However, devices using modulation doped wires require careful contact alignment that will make device scaling challenging. Furthermore, devices made using ion implantation require a high-temperature annealing step to activate the dopants. In Chapter 6, analysis of a nanowire FET fabricated by selective surface etching will be presented. This design addresses both the contact resistance limitation and the alignment and annealing concerns.

2.5. Summary

Silicon nanowires of high crystalline quality and controllable dimensions can be readily synthesized using the VLS growth mechanism. It has been demonstrated that *in situ* dopant incorporation and modulation doping are possible, confirmed by electrical characterization. However, studies reporting compositional analysis of impurity concentrations have been scarce because of the exceptionally high sensitivity required for such measurements. It is likely that, at least for the foreseeable future, chemical analysis of trace impurities in nanoscaled materials will remain an expensive and time-consuming task making it an impractical route to materials optimization. Instead, the utilization of these techniques to draw quantitative correlations with detailed electrical characterization of nanowire devices may lead to new models enabling accurate parameter extraction without the need for chemical analysis. Currently, nanowire doping levels are often estimated based on device performance and assumptions from the bulk and thin film literature.

This approach often leads to oversimplified and inaccurate results. With the exception of four-probe analysis of average resistivity, there are still few methods for accurately determining electronic properties of semiconductor nanowires. SPCM has been demonstrated as a quick and relatively simple way to qualitatively identify composition modulation in nanowire devices. In this work, advances in the analysis of SPCM and EBIC data are presented to establish quantitative relationships between the resulting photocurrent profiles and material properties such as minority carrier diffusion length and effective carrier concentration.

CHAPTER 3

Experimental setup and procedures

This chapter contains information about the equipment and experimental procedures utilized in the course of this work. Included are those procedures that were based on standard methods. In cases where new methods were developed, additional details will be presented in the results chapters.

3.1. Device fabrication

For the study of transport properties of individual semiconductor nanowires, it is necessary to interface macro-scale measurement equipment with nanometer-scale components. This was accomplished through a series of lithography steps to fabricate progressively smaller metallic features. The smallest of these are contacts to the nanowires themselves defined by electron beam lithography (EBL).

In chronological order, the process for nanowire device fabrication was as follows. First, heavily doped Si (100) substrates with a thin dielectric layer (400 nm SiO_2 or 200 nm Si_3N_4) were patterned with large electrodes via photolithography and subsequent metal evaporation. A grid pattern used for nanowire location defined by either photolithography or EBL is fabricated in the middle of the large electrodes. Figure 3.1a shows a typical photolithography pattern for substrate preparation. For the grid pattern and large electrodes, the metal deposition consisted of 5 nm of Cr followed by 50 nm of Au. The Cr layer acts as an adhesion layer between the Au film and the dielectric layer.

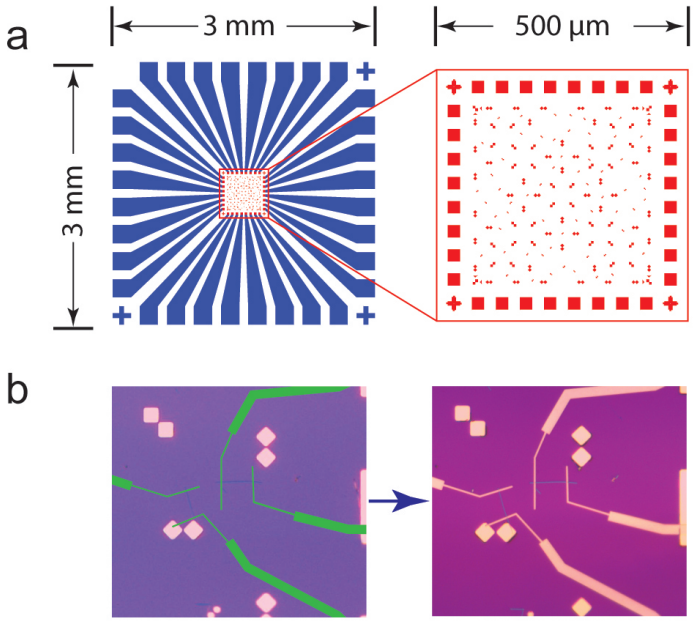

Figure 3.1. Nanowire device alignment and contact design. (a) Photolithography pattern and dimensions for a typical device substrate. (b) First image shows the location of two nanowires and contacts designed in CAD software. Second image shows the completed devices after EBL.

Next, nanowires were suspended in solution by sonicating (70 V, ~10 seconds) the growth substrate submerged in isopropyl alcohol. The nanowires in solution were then deposited on the prepared substrates and imaged using an optical microscope. The images were used to establish the position of the nanowires with respect to the existing grid so that electrodes could be designed with high accuracy. With the positions of the wires known, electrodes were drawn in CAD software to define an EBL pattern which was then written on the sample.

Electron beam resist must be deposited on the sample before EBL; however the order in which the resist was deposited depended on the sample. For wires with diameters of 30

nm or greater, the resist layer was put down prior to imaging on the optical microscope. It was found that the spin-coating process can sometimes move the wires so that spin-coating after imaging can result in misaligned contacts. This was particularly prevalent when working with larger diameter wires. However, reduced visibility through the resist layer made it nearly impossible to see wires with diameters of 20 nm or less, so imaging had to be done before spin coating. The electron beam resist used for nanowire device samples consisted of a bi-layer structure with a thin (~100 nm) polymethylmethacrylate (PMMA) layer on top of a thicker (~500 nm) methylmethacrylate (MMA) co-polymer layer. The PMMA layer is a high-resolution resist capable of features down to 10 nm while the MMA layer provides a thick undercut layer to assist in lift-off after metalization.

Up until this point, the fabrication procedure is largely material independent and should not change when contacting different types of nanowires. However, after developing the EBL pattern, the sample must be prepared for contact deposition which can include removal of the native oxide and residual polymer resist. The insulating surface oxide may act as a tunnel barrier between the contact and the wire resulting in nonlinear I-V behavior. A wet chemical etch or reactive ion etch can be used to remove the native oxide depending on the material; however, careful selection of the etch procedure is necessary to prevent deformation of the polymer mask and significant etching of the dielectric layer. Oxide regrowth is also a concern which can be addressed using surface passivation or by reducing exposure to oxygen after oxide removal. For all samples, residual polymer resist was removed using an oxygen or argon plasma cleaning step. Polymer on the sample surface can lead to poor adhesion of the contact metal or reduced interface quality between the contact and the nanowire.

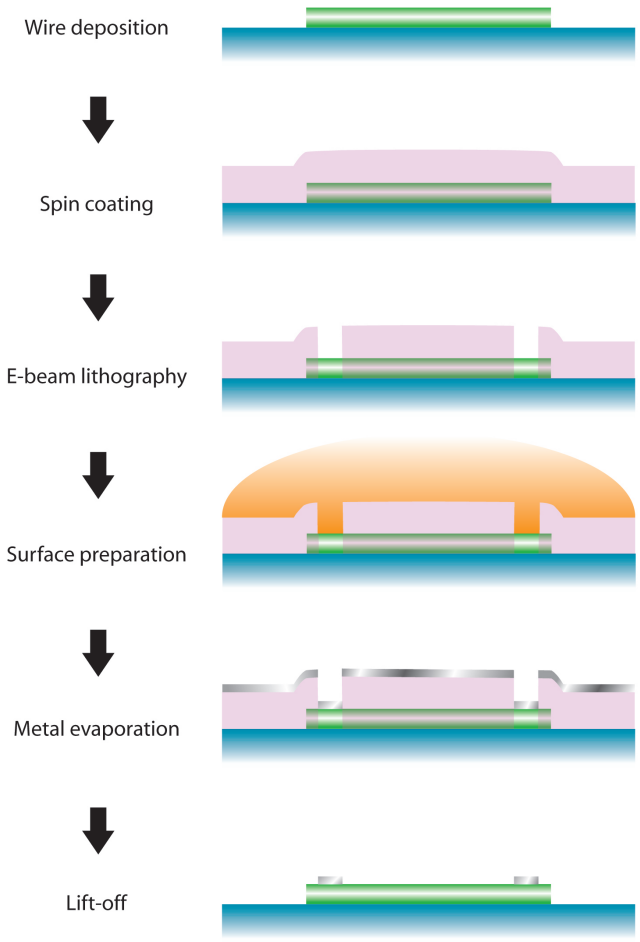

Figure 3.2. Nanowire device fabrication process flow.

After the etching steps, the metal electrodes are deposited using either a thermal or electron beam evaporator. Figure 3.1b shows a final device after deposition of metal contacts. If Ohmic contacts are desired, choice of metal for this step should be such that the resulting Schottky barrier is minimized (i.e. the work function of the metal should be less than that of the semiconductor). Finally, annealing may be necessary to improve interface quality at the contact or to form an intermediate phase.

Throughout the course of this work contacts have been fabricated to InAs, CdS, n-type Si, and p-type Si nanowires. Specific conditions for each are detailed in the following section.

3.1.1. Material specific surface preparation and contact metalization

For the case of CdS and Si the creation of both Ohmic and Schottky contacts will be discussed. Specific conditions for nanowire growth will not be included in this section, but can be found in Appendix C. For the purpose of this discussion Ohmic contacts are defined as contacts with negligible contact resistance compared to the resistance of the nanowire under study. Schottky contacts are those in which the Schottky barrier created at the metal-semiconductor junctions dominate transport in the device.

3.1.1.1. CdS. CdS nanowires used in this work were synthesized using low-pressure chemical vapor deposition (CVD) with a metalorganic powder source precursor and Au catalyst particles. Wires were undoped but displayed n-type character from I-V_G measurements. For all contacts to CdS, a 5 to 10-second wet chemical etch with buffered hydrofluoric acid (Buffer-HF Improved from Transene Company, Inc.) followed development of the EBL resist to remove the insulating oxide layer in the contact regions. Schottky contacts are readily formed by evaporation of Ti after etching.

Fabrication of Ohmic contacts to CdS requires increased doping in the contact region in order to narrow the Schottky barrier to promote tunneling of charge carriers across the junction. This was achieved by *in situ* Ar ion bombardment in the evaporator vacuum chamber followed by Ti evaporation. The evaporator chamber was first pumped down to ~$1x10^{-6}$ mbar before slowly bleeding in ultra-high purity Ar gas to bring the pressure to

$1.9x10^{-1}$ mbar. The sample stage was then biased to 500 V using a DC power source (MDX 1K from Advanced Energy) and the output was run through an arc suppression unit (SPARC-LE, Small Package Arc Repression - Low Energy, from Advanced Energy) to prevent arc discharges during bombardment. The large field present near the sample stage created an Ar+ plasma and because the sample was attached to one of the electrodes the charged ions are accelerated at the sample and cause damage to the crystal structure.

The ion bombardment preferentially creates sulfur vacancies in the crystal which act as donors and increase the equilibrium electron concentration in the exposed regions of the nanowire[69,70]. The above procedures were used to reliably create Ohmic devices consisting of two Ar ion bombarded contact regions and Schottky diode devices in which only one of the two contact regions was bombarded.

3.1.1.2. InAs. InAs nanowires used in this work were synthesized using low-pressure chemical vapor deposition (CVD) with trimethylindium and arsine sources and Au catalyst particles. Wires were undoped but displayed n-type character from I-V_G measurements. For all contacts to InAs, the insulating oxide layer in the contact regions was removed during a 5 to 10-second wet chemical etch with buffered hydrofluoric acid after developing the EBL resist.

As with the CdS wires, fabrication of Ohmic contacts to InAs required *in situ* Ar ion bombardment of the contact region. The mechanism for reduced contact resistance of InAs is not known, but it may be similar to the CdS case. Following Ar ion bombardment, evaporation of Ni yielded ohmic contacts to the InAs nanowires.

3.1.1.3. n-Si. Si nanowires used in this work were synthesized using low-pressure chemical vapor deposition (CVD) with vapor-phase precursors and Au catalyst particles. Wires

doped with phosphorous displayed n-type character from I-V_G measurements. For all contacts to Si, a 30-second O_2 plasma clean was used to remove residual organic material prior to wet chemical etching with buffered HF to remove the native oxide layer. Ohmic contacts were fabricated by evaporating Ni immediately after etching. However, it was found that contact resistance increases sharply with decreasing doping level. In order to achieve Ohmic contacts, very heavily doped wires must be used so that the depletion width of the Schottky barrier is sufficiently small that electrons can tunnel across the junction efficiently.

3.1.1.4. p-Si. P-type Si nanowires were synthesized by doping with boron during VLS growth. Contact fabrication procedures were identical to the n-type Si nanowire contacts with the exception of an additional annealing step after contact deposition. As with the n-type wires, Ohmic contacts to p-Si require heavy doping to narrow the Schottky barrier. However, Si nanowire growth in the presence of diborane (the source used for boron dopants) often results in heavily tapered structures as diborane assists in the decomposition of the silicon source. For this reason it is desirable to use lightly doped wires which have less taper. In order to lower the contact resistance in p-type Si nanowire with low doping, samples were annealed after Ni deposition to form a Ni_xSi_{x-1} phase. Ni diffuses into the Si forming a silicide which can be seen in SEM (Figure 3.3). Annealing was conducted at atmospheric pressure in forming gas. Samples were first held at 125 °C for three minutes then rapidly heated to 450 °C using two IR lamps for 30 seconds to 1 minute and then allowed to cool. This type of contact to silicon nanowires has been demonstrated previously with great control over intrusion length[25,71,72].

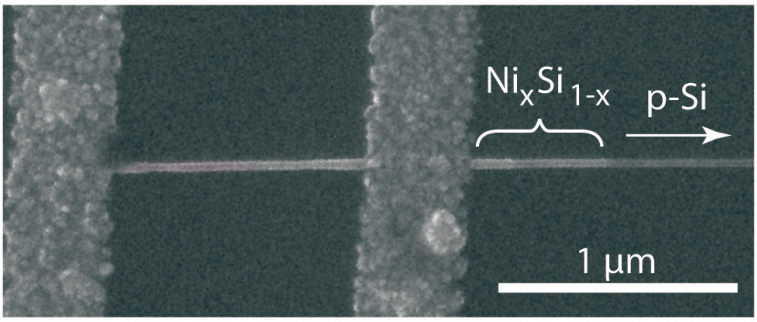

Figure 3.3. SEM image of an intruded silicide contact in a p-Si nanowire.

3.2. Standard device characterization

All measurements were made on an MMR Variable Temperature Micro Probe probe station using custom designed software (Labview 7.0) allowing for measurement of analog voltage signals by the operating computer. Analog voltage outputs are supplied by a National Instruments DAQ board capable of ± 10 V signal output. For voltage measurements, analog voltage inputs on the DAQ board are used which are capable of ± 10 V input signal measurement. Currents are measured by using a current pre-amplifier to convert current signals to a voltage before being recorded by the computer through the DAQ board. The system is capable of measuring sub-pA currents. For increased accuracy and reduced noise level, each data point is an average of multiple measurements. The number of measurements can be set in the software.

3.2.1. Four-probe analysis: Contact resistance and resistivity

In many cases the characterization of electronic properties of semiconductor nanowires necessitates device integration. However, this poses an additional challenge as one must ensure that measured properties are indeed a property of the nanowire itself and not

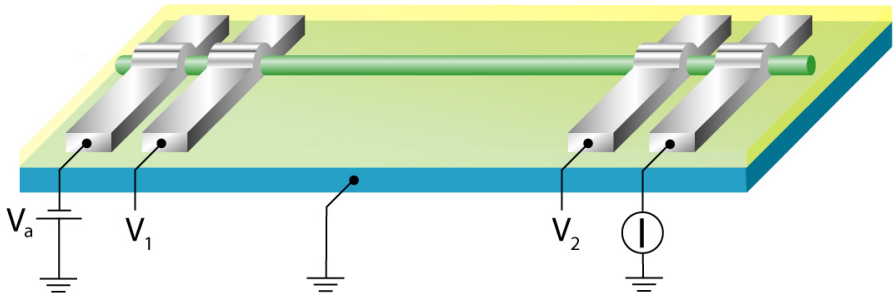

Figure 3.4. Schematic of a four-probe nanowire device.

influenced by its integration into a device. For example, resistance measurements of two-terminal nanowire devices cannot be used to accurately determine the resistance of the nanowire unless the contact resistance is known. Four-probe device geometries are commonly used to remedy this problem and can be used to quantitatively determine the total series resistance introduced by the contacts as well as the nanowire resistivity. Figure 3.4 shows a schematic of a four-probe nanowire device. Determination of the nanowire resistance is made by applying a bias across the outer contacts and measuring the device current while measuring the potentials at the inner contacts, V_1 and V_2. By Ohm's law the resistance of the nanowire, R_{NW}, is given by Equation 3.1.

$$R_{NW} = \frac{V_1 - V_2}{I} \tag{3.1}$$

The resistance is related to the resistivity, ρ, by $R = \frac{\rho L}{A}$ where L is the device channel length and A is the cross-sectional area. The channel length is defined by the contact spacing and cross-sectional area can be determined by measuring the wire diameter using

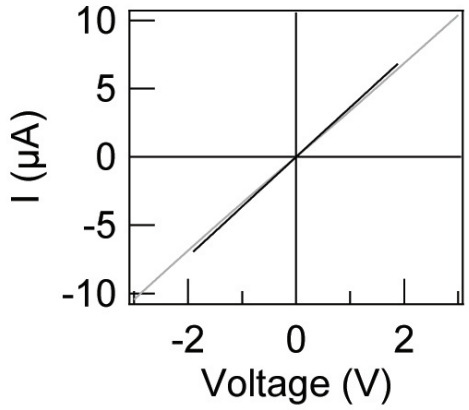

Figure 3.5. Four-probe (black) and two-terminal (red) I-V data for an n-Si nanowire device. From this plot the total series resistance introduced by the contacts is 16 kΩ.

SEM or AFM. If the cross-sectional area is constant across the entire device then calculation of the resistivity is straight-forward. This type of analysis enables the comparison of nanowires without complication from variability in contact resistance and is necessary to quantitatively compare wires of different doping levels for which the contact resistance can differ greatly. However, this approach yields only an average resistivity and therefore cannot account for non uniformities within the wire. Also it is assumes that the full cross section of the wire contributes to conductivity when in fact there may be a surface depletion layer[49,58]

Furthermore, the series resistance introduced by the metal contacts can be quantitatively determined by comparing the four-probe measurement with a two-terminal measurement. Figure 3.5 shows data from a four-terminal n-Si nanowire device for which the two-terminal resistance is 291 kΩ and the nanowire resistance from four-probe analysis is 275 kΩ. This gives a total contact resistance of 16 kΩ which is 5.5 % of the total two-terminal resistance. It is important to note that this value is the total series resistance

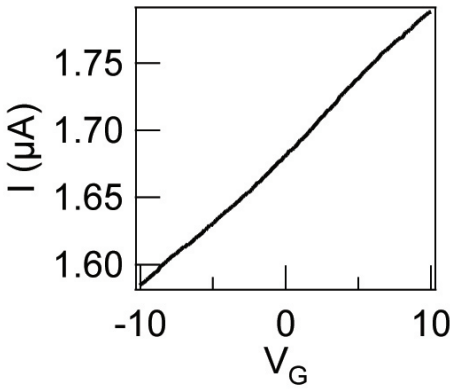

Figure 3.6. Transfer curve for a heavily doped n-Si nanowire device. The field-effect mobility estimated from this device is 38 cm^2/V-s.

introduced by the two contacts and that it is not possible to determine the resistance of each contact independently by this method.

3.2.2. Field-effect mobility

To date, a direct quantitative approach to measuring the mobility of electrons and holes in semiconductor nanowires has not been reported. Instead, the field-effect mobility, μ_{FE}, is commonly used as an indicator of the true carrier mobility. Typical two-terminal nanowire devices are fabricated on top of heavily doped Si substrates coated with a thin dielectric layer. In this case the substrate can act as a gate electrode to apply an external electric field to modulate the carrier concentration in the nanowire. The device transfer curve can be obtained by measuring the device current as a function of the back gate voltage. An example of a transfer curve for a heavily doped n-Si nanowire device is given in Figure 3.6. The field-effect mobility is given by

$$\mu_{\mathrm{FE}} = \frac{\mathrm{dI_{DS}}}{\mathrm{dV_G}} \times \frac{\mathrm{L}^2}{\mathrm{C_{ox}}} \times \frac{1}{\mathrm{V_{DS}}} \tag{3.2}$$

Here dI_{DS}/dV_G is the slope of the linear portion of the transfer curve, L is the device channel length, V_{DS} is the applied drain-source bias, and C_{ox} is the oxide capacitance. The oxide capacitance is too small to measure and therefore needs to be estimated based on the device geometry and material parameters. In the literature, a commonly used approximation for the oxide capacitance is taken from the metallic cylinder-plane model which gives the expression:[50,73,74]

$$C_{ox} = \frac{2\pi\epsilon_0\epsilon_r L}{\cosh^{-1}\left(\frac{r+t_{ox}}{r}\right)}$$

where ϵ_r is the dielectric constant of the gate dielectric, t_{ox} is the dielectric thickness, and r is the nanowire radius. However, it was recently reported by Khanal and Wu[75] that this expression is only applicable if the cylinder is buried in the dielectric. In this report, it was shown that for the typical back-gated nanowire device structure the resulting capacitance is overestimated by a factor of 2. Therefore the correct expression becomes:

$$C_{ox} = \frac{\pi\epsilon_0\epsilon_r L}{\cosh^{-1}\left(\frac{r+t_{ox}}{r}\right)}$$

For the device presented in Figure 3.6 the estimated gate capacitance is 9.4×10^{-16} F. Combining this with known values, Equation 3.2 gives a field-effect mobility of 38 cm^2/V-s.

It must be stressed that this value is not the true carrier mobility but rather a figure of merit for transistor performance. Given an accurate estimate of the gate capacitance it is expected that the field-effect mobility will be close to the true mobility. However, the approach detailed above involves approximations and assumptions that cause the resulting value to deviate significantly from the actual mobility.

3.3. Scanning photocurrent microscopy (SPCM)

In scanning photocurrent microscopy (SPCM) a diffraction limited laser spot is rastered in two dimensions over a device area while changes in device current are measured as a function of beam position. In this work, SPCM has been used to investigate doping in Si nanowires (Chapter 5), identify operating principles of nanowire FETs (Chapters 6 and 7), and study nanoscale metal-semiconductor junctions (Chapter 8). The details of those findings will be given in later chapters. This section details the implementation and operating procedures involved in SPCM measurements.

3.3.1. Equipment setup and procedures

With the exception of the measurements on InAs nanowires presented in Chapter B, all SPCM measurements were made on a Witec Alpha300 confocal microscope with a piezoelectric scanning stage. A schematic of the experimental setup is shown in Figure 3.7. A custom sample holder was fabricated using standard printed circuit board (PCB) techniques. Samples were mounted to the PCB using carbon tape and devices were bonded to the copper electrodes with a wedge-bonder using aluminum wire. With the sample in place, the PCB holder was placed on the scanning stage and held down with spring clips. The sample holder was terminated at a 9-pin d-sub miniature connector that was used to interface with a custom BNC switch box. This box allowed all of the bonded devices to be grounded when they were not being measured to prevent unintentional charge buildup that might discharge and burn out the nanowire devices. The device under study was then hooked up to external electronics using BNC terminated coaxial cables.

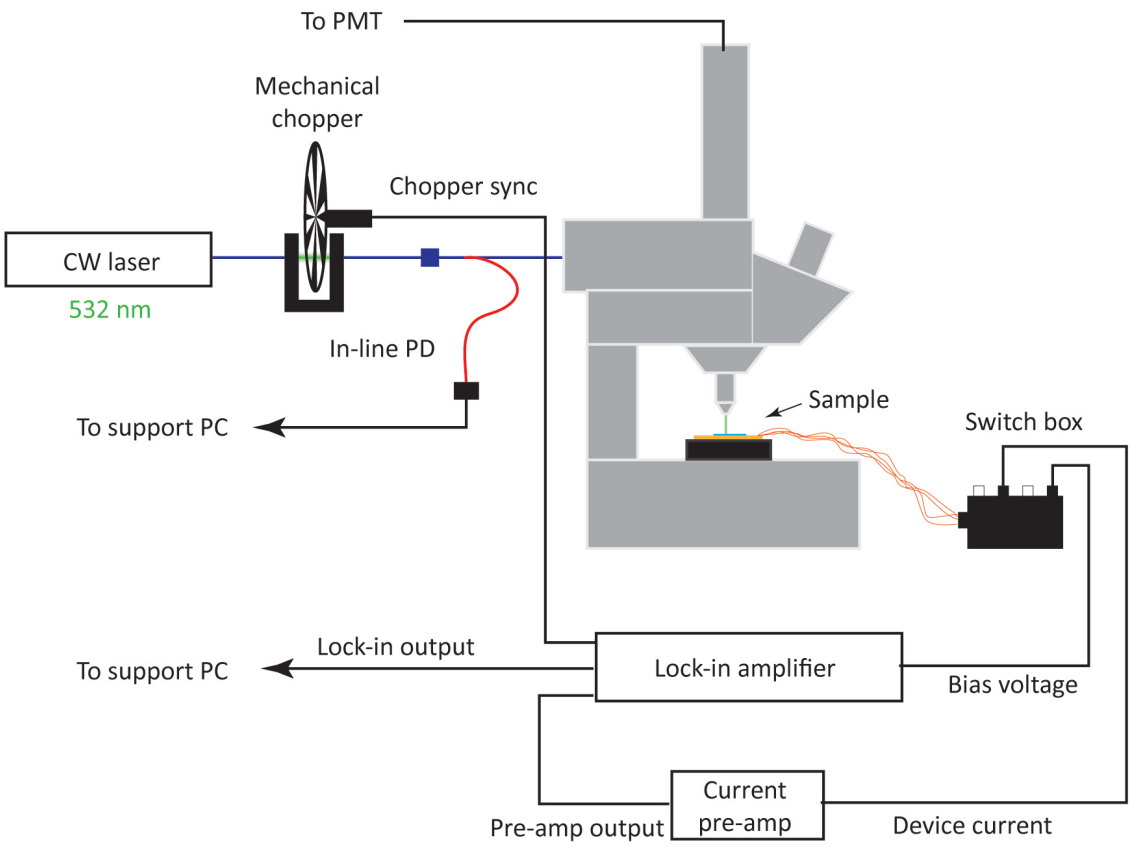

Figure 3.7. Schematic of the experimental setup for SPCM measurements.

A polarized continuous-wave 532 nm fiber-coupled light source was focused to a diffraction limited spot using a 100x confocal microscope objective while the sample was translated using the scanning stage. In all cases the samples were oriented such that the device channel was aligned parallel with the direction of polarization. When illuminated, any change in device current was measured and correlated with the location of the laser spot. As the sample was scanned a two-dimensional photocurrent map was created.

Depending on the device in question, the photocurrent signal can be quite small necessitating very low noise levels. To improve the signal-to-noise ratio in our measurements, a mechanical chopper was used to chop the illumination at a set frequency and the induced current was measured using a Signal Recovery lock-in amplifier. The chopper blade was introduced between the laser source and the confocal microscope's coupler unit using a pig-tail style U-Bracket from OzOptics. This provided ˜1.5 inches of free-space in the otherwise completely enclosed beam path. An in-line fiber tap with integrated Si photo diode was used to monitor the laser intensity during the measurement. Calibration was such that the photo diode reading corresponded to the laser power just before the microscope objective. It is expected that an additional 2 to 5 % of the laser intensity was lost in the objective. Devices were biased using the analog voltage outputs of the lock-in. The chopped excitation gave rise to a small AC current on top of a potentially large DC background (depending on the sample). The AC component can be isolated using a lock-in amplifier that will filter out the DC background as well as any periodic noise that is not at the measurement frequency. The current signal from the device was first amplified and converted to a voltage using a current preamplifier. The voltage signal was then connected to the channel input of the lock-in amplifier which was syncronized to the chopper frequency. The in-phase signal output of the lock-in was recorded on the auxilary input of the Witec control hardware so that it could be collected concurrently with other signals while scanning. Full scale signal of the auxilary input is $\pm$ 10 V.

Lock-in amplifiers typically report both the in-phase and out-of-phase components of the signal at a given frequency. Alternatively these signals can be combined to give the total magnitude of all oscillations at the oscillator frequency. The best signal-to-noise

ratio is obtained when only the in-phase component of the signal is recorded as this avoids external sources of noise that may happen to be near the measurement frequency. To ensure that the phase of the lock-in was in-phase with the induced current signal, the beam was positioned over the device at a location with relatively high photocurrent while the built-in auto phasing function of the lock-in was used to set the phase. It was found that the phase offset changed every time the chopper was turned on and off, so it was necessary to reset the phase when the chopper settings were changed.

An optimal frequency for this type of measurement is one that is far from any detectable periodic sources of noise. The frequency for SPCM measurements in this work was selected by finding a quiet frequency in the Fourier transform of the DC current signal monitored by a digital oscilloscope. With the exception of those in Chapter B, all SPCM measurements were conducted at 1919 Hz corresponding to a period of ~0.5 ms. The time constant of the lock-in output filter was set to 5 ms so that the measured amplitude of the AC signal was averaged over multiple periods. Furthermore, the dwell time for each point in the SPCM data was 15 ms thus further reducing the noise.

3.4. Electron beam induced current (EBIC)

Electron beam induced current (EBIC) measurements are analogous to SPCM in that they involve rastering a focused beam over a device while measuring changes in device current. The difference in this case is that EBIC is done inside an SEM using the electron beam to excite excess carriers in the semiconductor. In Chapter 4 the application of EBIC to quantitatively measure short minority carrier diffusion lengths in n-Si nanowires

is presented. This section details the implementation and operating procedures involved in EBIC measurements.

3.4.1. Equipment setup and procedures

As with SPCM, EBIC involves the measurement of potentially very small signals, so a lock-in amplifier was used to improve the signal to noise ratio. EBIC measurements were conducted using an FEI Quanta E-SEM. A schematic of the experimental setup is shown in Figure 3.8. This SEM has EBL capability and therefore has a high-speed beam blanker that is externally controlled. By utilizing this feature it was possible to modulate the electron beam at an arbitrary frequency simply by driving the beam blanker with a 3.5 V sine wave provided by the internal oscillator of the lock-in amplifier. Electrical feedthroughs on the vacuum chamber were used to measure device current *in situ*. A custom sample holder like the one used for SPCM was made using a PCB with a 14-pin ribbon cable connector termination. Outside of the vacuum chamber a 14-pin ribbon cable connected the feedthrough to a BNC switch box. The applied bias was supplied by the voltage output of the lock-in amplifier and current was measured by converting the current to a voltage using a current pre-amplifier and filtering out the DC background and noise using the lock-in amplifier. Control of the electron beam and signal recording was done using the Nanometer Pattern Generation System (NPGS) EBL software. In order to record the EBIC signal, the in-phase signal output of the lock-in was connected to the intensity input on the NPGS computer which is capable of recording a $\pm$ 10 V signal. The NPGS computer is only able to record one signal at a time, so it was not possible to concurrently measure the detector signal and the induced current signal. Therefore

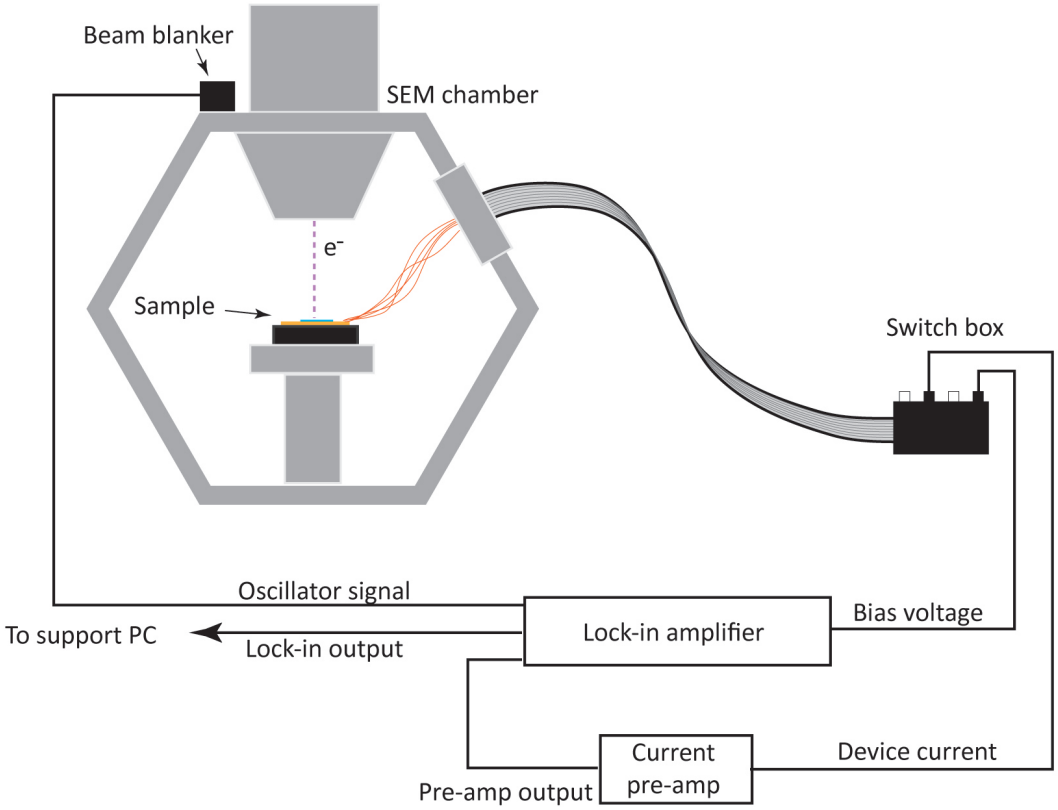

Figure 3.8. Schematic of the experimental setup for EBIC measurements.

comparisons of SEM images with EBIC maps must be done using sequentially acquired images.

The 'Digital Imaging' function of the NPGS software is used to define the scanning parameters as well as capture the signal. The magnification should be set based on the last magnification used in imaging mode, and the scan resolution should be selected to minimize exposure to the beam while still providing sufficient spacial resolution for the feature of interest. The dwell time per point is changed by setting the number of readings taken at each point. Each reading takes 2.7 μs, so for a dwell time of 20 ms this should be

~7400 readings per point. The frequency used for EBIC measurements was determined in the same way as for SPCM measured and was also 1919 Hz.

Because of the potential for beam damage and carbon deposition during EBIC, precautions were taken to minimize exposure. Imaging of the devices was kept to a minimum, and scan resolution and dwell time set to their minimally required values. For the data presented in Chapter 4, typical imaging conditions were a 5 ms lock-in time constant, 15 ms dwell time, and 100×100 scan resolution taken at $>$ 90,000× magnification. Furthermore, the auto phasing procedure practiced for SPCM measurements could potentially damage the device as it involves holding the beam in one location for an extended period of time. Instead, the phase offsets were determined by using the output of the internal oscillator to drive an AC current signal through a nanowire device. The current was then measured in the same way that the EBIC signal is measured and the phase offset was determined by auto phasing the lock-in. The phase offset from the current pre-amplifier increases with increasing sensitivity setting. This approach worked for EBIC because the fast beam blanker on the SEM does not introduce an appreciable phase shift at the relatively low frequencies used for the measurement. This method does not work for SPCM because of the changing phase shift introduced by the mechanical chopper. It was found that the determined phase offset values do not change significantly across multiple devices provided that the contact resistance is low and the wires are fairly conductive. In devices fabricated with very resistive nanowires ($>$ 100 MΩ), it was not possible to measure an AC signal through the device due to the large displacement current which produced an out-of-phase signal.

3.5. Summary

The procedures discussed in this chapter were utilized routinely throughout this work in the fabrication and analysis of nanowire devices. The rest of the document focuses on results and development of new techniques and will therefore omit unnecessary repetition of information contained here.

CHAPTER 4

Quantitative determination of hole diffusion lengths in n-Si nanowires using EBIC

The minority carrier diffusion length is a transport property of an extrinsic semiconductor that gives the average distance excess minority carriers can diffuse before recombining and is given by

$$\mathrm{L_p} = \sqrt{\mathrm{D_p}\tau_\mathrm{p}} \tag{4.1}$$

where L_p is the diffusion length of holes in an n-type semiconductor, D_p is the diffusivity, and τ_p is the lifetime. The design and optimization of minority carrier devices such as p-n diodes, light-emitting diodes, and solar cells depend critically on L_p. Specifically, in solar cells carrier generation occurs as light is absorbed throughout the device structure. However this only results in electrical power generation if the excess minority carriers are collected at an internal junction in the structure. Therefore it is important to maximize the diffusion length in order to efficiently collect the excess charge. From Equation 4.1 we see that L_p is sensitive to carrier lifetime and diffusivity both of which are strongly dependent on impurity concentrations and crystal defects making the diffusion length an indicator of crystal quality. For traditional solar cells this means that exceptionally high quality materials are required leading to increased cost. Recently a novel structure for nanowire-based solar cells was proposed which could potentially allow for enhanced

efficiency with lower quality materials[76]. In a detailed device performance analysis it was found that the optimal nanowire diameter for such a structure is one which is equal to the minority carrier diffusion length. For the purpose of the analysis a bulk-like value of L_p was assumed; however no measurement of diffusion lengths in nanowires had been reported at that time.

In this chapter quantitative measurements of hole diffusion lengths in n-type silicon nanowires will be presented. Using EBIC (see section 3.4 for experimental setup) it was found that L_p increased monotonically with nanowire diameter indicating a strong influence from surface recombination. Comparison of the diameter dependence with modeled results indicated a high density of interface states likely caused by incomplete passivation of surface states by the native oxide. Furthermore attempts to extend the diffusion length using dry oxidation to improve the interface were unsuccessful. This may be an indication that the high curvature of the nanowire surface prevents the formation of a high quality interface.

4.1. Measurement principles and diffusive transport of excess carriers in 1-D

In the following discussion the principle of minority carrier diffusion length measurements in nanowire devices using EBIC will be detailed. In EBIC, a focused electron beam is used to excite excess carriers in a semiconductor device while changes in current are recorded as a function of the beam position. By first explaining the expected excess carrier distribution, the minority carrier diffusion length measurement becomes relatively straightforward.

The behavior of nonequilibrium excess carriers in semiconductors can be described by the ambipolar transport equation. Upon injection of a nonequilibrium population of electrons and holes in the semiconductor, the carriers will diffuse due to the introduced concentration gradient and will drift in any electric fields present. The ambipolar transport equation takes into account the internal field created when the excess electrons and holes are separated that attracts the carriers back together. In the limits of extrinsic doping and low carrier injection the transport parameters of both carrier types reduce to the minority carrier values and the one-dimensional ambipolar transport equation becomes

$$\mathrm{D_p}\frac{\partial^2(\delta \mathrm{p})}{\delta \mathrm{x}^2} - \mu_\mathrm{p}\mathrm{E}\frac{\partial(\delta \mathrm{p})}{\delta \mathrm{x}} + \mathrm{g} - \frac{\delta \mathrm{p}}{\tau_\mathrm{p}} = \frac{\partial(\delta \mathrm{p})}{\partial \mathrm{t}} \tag{4.2}$$

where μ_p is the hole mobility, E is the electric field, g is the carrier generation rate, and δp is the excess hole concentration. If we now consider the steady-state population of excess holes in an n-type semiconductor with no external electric field, we find that at the point of injection Equation 4.2 reduces to

$$\mathrm{g} - \frac{\delta \mathrm{p}}{\tau_\mathrm{p}} = 0 \quad \text{or} \quad \delta \mathrm{p} = \mathrm{g}\tau_\mathrm{p} \tag{4.3}$$

Therefore in the excitation region the excess hole population is constant and equal to $g\tau_p$. Beyond this point there is no excess carrier generation, so $g = 0$, and diffusion of holes must now be considered. In this region the ambipolar transport equation becomes

$$\mathrm{D_p}\frac{\partial^2(\delta \mathrm{p})}{\delta \mathrm{x}^2} - \frac{\delta \mathrm{p}}{\tau_\mathrm{p}} = 0 \tag{4.4}$$

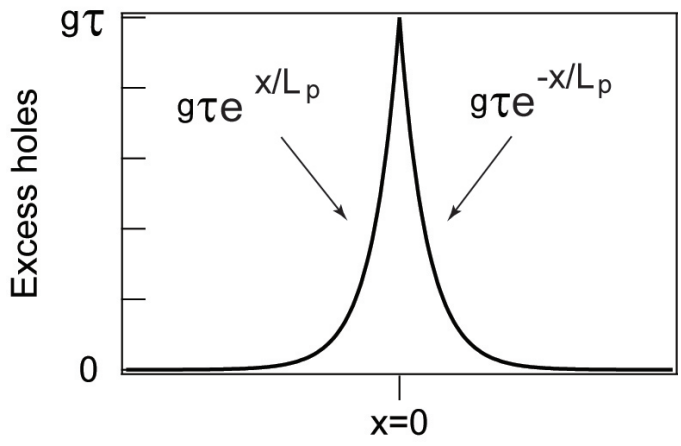

Figure 4.1. Calculated excess hole concentration vs position. Excitation at $x = 0$ creates a steady state population of $g\tau$ which decays exponentially with decay constant L_p when no external electric field is present.

Using Equation 4.1 this can be rewritten as

$$\mathrm{L_p^2}\frac{\partial^2(\delta \mathrm{p})}{\delta \mathrm{x}^2} - \delta \mathrm{p} = 0 \tag{4.5}$$

Using the boundary condition that at $x = \pm\infty$ the excess carrier concentration decays toward zero the solution to Equation 4.7 is

$$\begin{aligned} \delta \mathrm{p} &= g\tau_p e^{-x/L_p} \quad x \geq 0 \\ \delta \mathrm{p} &= g\tau_p e^{x/L_p} \quad x \leq 0 \end{aligned} \tag{4.6}$$

Therefore in the absence of an electric field the excess carrier concentration will decay away from the point of excitation as a single exponential with characteristic decay constant, L_p, as shown in Figure 4.1.

From the above discussion, it can be concluded that the EBIC signal will be zero in the absence of an electric field as electrons and holes will diffuse equally in both directions and

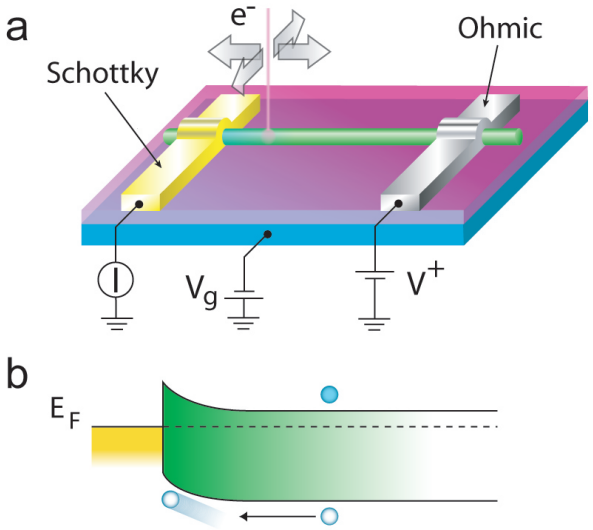

Figure 4.2. Schematic of EBIC measurement of a nanowire Schottky diode. (a) Diagram of a nanowire Schottky diode under reverse bias. (b) Band diagram showing excitation of excess carriers and diffusion of holes to the space-charge region.

will therefore not result in a current. For the measurement of L_p, Schottky diode devices are used so that the internal electric field at the Schottky barrier can be used to collect excess minority carriers (see Figure 4.2). In this case excess minority carriers created close to the junction will be collected giving rise to an EBIC signal. As the excitation source (electron beam) is moved away from the Schottky junction the current will decrease as fewer holes are able to diffuse to the junction until the excitation is sufficiently far from the junction that no current is measured. The resulting current profile should therefore be proportional to the minority carrier distribution given by Equation 4.6. This approach has been used for the determination of minority carrier diffusion lengths in bulk and thin film crystals[77] where it is found that the decay is not a single exponential and typically requires a correction factor of $x^{3/2}$. This factor is related to the shape of the generation

region which is roughly spherical below the surface of the material. In the case of a nanowire device, the majority of the excitation beam will pass through the semiconductor without scattering while only a small fraction of the incident electrons will actually scatter and create excess carriers. For this reason the generation region will not be significantly larger than the excitation beam and will instead be limited by the dimensions of the nanowire itself. Therefore it is expected that the decay of the EBIC signal away from the Schottky junction will be directly proportional to the excess hole distribution, or

$$I_{EBIC} \propto e^{-x/L_p} \tag{4.7}$$

Figure 4.3 shows EBIC data from an n-Si nanowire Schottky diode. The bright contrast in the EBIC image of Figure 4.3b indicates an increase in device current. From the image it is seen that there is a maximum in the induced current signal close to the Schottky contact which decays along the nanowire axis. Line profiles taken along the nanowire axis show a single exponential decay while those taken across the nanowire show an abrupt drop off in signal confirming that there is little influence from secondary electrons. From this data, L_p can be determined by fitting the decay of the current to an exponential to obtain the decay constant.

4.2. Hole diffusion length versus wire diameter

Nanowire Schottky diodes were fabricated using phosphorous-doped silicon nanowires of various diameters and doping levels. Devices were made with one nickel contact (Ohmic) and one gold contact (Schottky) using serial electron beam lithography steps. It was found that the hole diffusion length shows a strong dependence on wire diameter increasing

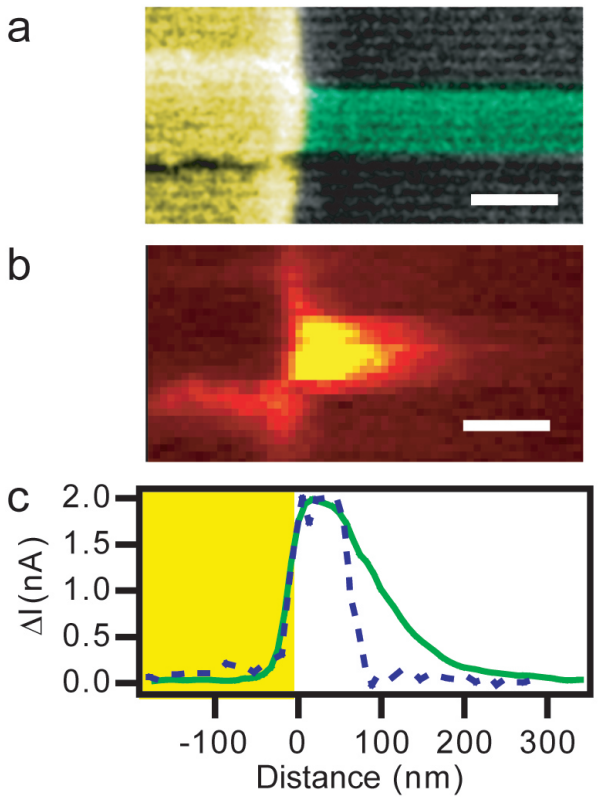

Figure 4.3. EBIC measurement of a nanowire Schottky diode. (a) False-color SEM image of the nanowire device near the Schottky contact. (b) EBIC signal from the region in 'a'. Bright contrast indicates an increase in current. (c) Line profiles of the EBIC data in 'b' taken along the nanowire axis (solid line) and across the nanowire (dashed line). Scale bars are 100 nm.

monotonically from 25 nm up to 80 nm for nanowires 30 nm to 100 nm in diameter, respectively. Figure 4.4 shows the exponential decay of line profiles of EBIC data taken from nanowire Schottky diodes of three different diameters where it is seen that the data for smaller wire diameters show a much faster decay. In contrast, the hole diffusion lengths in bulk n-type Si at comparable doping levels ($\tilde{}1 \times 10^{19} - 1 \times 10^{20} cm^{-3}$) are 1-10 μm indicating a 100 to 1000-fold decrease in nanowires compared to the bulk. This dramatic

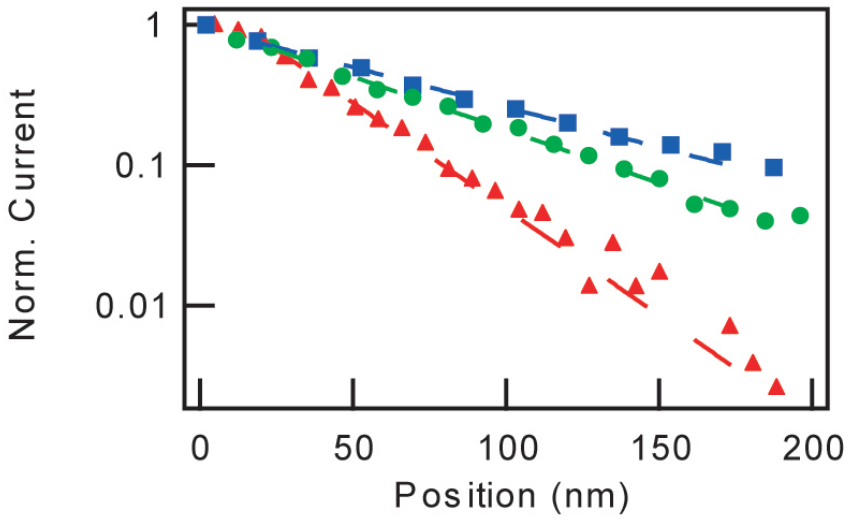

Figure 4.4. Semi-logarithmic plot of normalized EBIC profiles for nanowires having diameters of 93 nm (blue squares), 55 nm (green circles) and 35 nm (red triangles) with minority carrier diffusion lengths of 78 nm, 57 nm and 28 nm respectively. The dashed lines are exponential fits to the data.

decrease in carrier diffusion lengths points to a significant decrease in either the carrier lifetime or the diffusivity. The strong diameter dependence rules out a significant role of impurities or other defects that might limit the diffusion length as these would not change with diameter. This is confirmed by measurements made on wires with varying doping levels (Figure 4.5). If charged impurity scattering dominated the minority carrier transport an increase in diffusion length would be expected for a decreased doping level. Therefore it is concluded that the minority carrier diffusion length in n-Si nanowires is limited by surface recombination. It should be noted that the minority carrier diffusion length is typically considered a material property and is measured away from the influence of the semiconductor surface. For this study we are interested in the diffusion length for a nanowire geometry and therefore the influence of the surface is a necessary component.

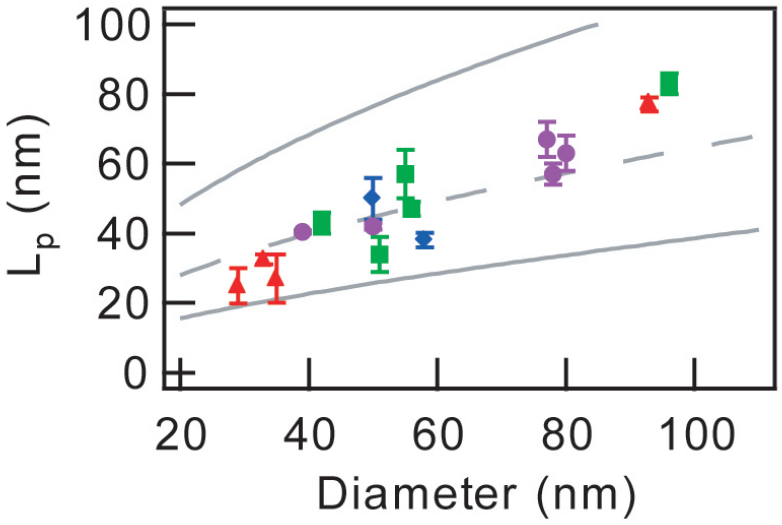

Figure 4.5. Plot of L_p versus diameter for varying gas-phase Si:P doping ratios: 500:1 (red triangles), 1000:1 (green squares), 1500:1 (blue diamonds), 2000:1 (magenta circles). Grey lines are model calculations of L_p vs diameter for various values of the surface recombination velocity, S. Top, bottom and dashed lines correspond to $S = 1 \times 10^5 cm\ s^{-1}$, $1 \times 10^6 cm\ s^{-1}$ and $3 \times 10^5 cm\ s^{-1}$, respectively.

The values reported here therefore represent an *effective* diffusion length that indicates the average distance excess holes will diffuse along the nanowire length before recombining at the surface.

4.3. Surface recombination velocity

To quantitatively account for the diameter-dependent diffusion length and to gain physical insight into the relative influence of surface and bulk recombination processes, a simple model of minority carrier diffusion and recombination was applied based on previous work on quantum dots[78]. As with the diffusion length we will define an *effective*

hole lifetime, $\tau_{p,eff}$, representing the average lifetime of excess holes in the nanowire accounting for surface recombination.

The diffusion of excess carriers to the surface of a nanowire and their subsequent recombination is formally equivalent to evaporation from the surface of a cylinder[79]. This analogy was first applied to surface recombination in semiconductor quantum dots by Daiminger et al.[78] The model assumes that both electrons and holes are present at the surface and that recombination is non radiative. The nanowires used for this study are heavily doped n-type so it is expected that any surface states will be occupied by electrons and that the population of electrons at the surface will always be in excess of the hole population. We therefore considering only the diffusion of minority holes to the surface. The effective carrier lifetime is given by:

$$1/\tau_{\mathrm{p,eff}} = 1/\tau_{\mathrm{p,s}} + 1/\tau_{\mathrm{p,B}}$$

where $\tau_{p,B}$ is the bulk hole lifetime and $\tau_{p,s}$ is the inverse of the rate of surface recombination. The effective lifetime can be determined by solving the continuity equation for the carrier concentration profile leading to the following expression:

$$1/\tau_{\mathrm{p,eff}} = (4\beta^2 \mathrm{D_p})/\mathrm{d}^2 + 1/\tau_{\mathrm{p,B}}$$

where D_p is the hole diffusion constant, d is the wire diameter, and β is given by

$$\beta \mathrm{J}_1(\beta) - \mathrm{L}\mathrm{J}_0(\beta) = 0, \quad \text{and} \quad \mathrm{L} = (\mathrm{dS}/2\mathrm{D_p})$$

where S is the surface recombination velocity and $J_{0,1}$ are Bessel functions of zero and first order respectively. By solving for the roots, β, of this transcendental equation, one can calculate the effective lifetime for a given nanowire diameter and surface recombination velocity. At the doping levels in the nanowires used for this study, the minority carrier mobility will be limited by ionized impurity scattering[80] suggesting that D_p, given by $D_p = \mu_p k_B T/q$ by the Einstein relation, will be comparable to the bulk value and that the diffusion length will be limited by the lifetime, $\tau_{p,eff}$, due to recombination at the surface.

Using the above relation, the curves bounding the data plotted in Figure 4.5 were generated. It was found that $S \approx 3 \times 10^5\, cm\ s^{-1}$. Using this value for S and the known capture cross-section for holes at the $Si - SiO_2$ interface[43], one can use the following equation to estimate an interface state density:

$$\mathrm{S} = \sigma_\mathrm{p} \mathrm{v_{th}} \mathrm{N_{it}} \tag{4.8}$$

Here σ_p is the capture cross-section for holes, v_{th} is the thermal velocity for holes, and N_{it} is the interface state density. This gives a value of ~$1.7 \times 10^{13}\, cm\ s^{-2}$, which is consistent with values reported for native oxide on Si[81].

It is worth noting that the plot in Figure 4.5 suggests that S is not strictly constant with diameter and instead is shown to decrease with increasing diameter. A reduced contribution from surface recombination at larger diameters may be interpreted physically as an improved interface quality for wires with larger diameter. Alternatively, it may be the excess carriers created in the bulk of the wire are affected by band bending at the

nanowire surface in which case a larger diameter may reduce the relative influence of these internal fields.

4.4. Silicon nanowire surface passivation

Having established that the minority carrier transport in silicon nanowires is dominated by surface recombination, efforts were made to extend the minority carrier diffusion length by passivating the nanowire surface. In principle, reducing the interface state density of the silicon would reduce the surface recombination velocity and increase the minority carrier diffusion length. Passivation was attempted both inorganically by dry oxidation and organically using octadecene functionalization.

Oxidation of silicon nanowires was achieved by annealing at elevated temperature in an oxygen partial pressure. As was discussed in Chapter 2, significant dopant activation has been observed in boron-doped silicon nanowires at temperatures as low as 800 °C. In order to avoid this issue, oxidation was performed at 650 to 700 °C based on conditions reported by Shir et al.[82]. Prior to oxidation, the gold catalyst particle was removed from the tips of the nanowires using a standard tri-iodide etchant solution followed by an RCA cleaning process. Removal of the catalyst was confirmed by SEM as shown in Figure 4.6. A series of oxidations were performed at either 650 or 700 °C with oxidation times of 30 to 90 minutes. Nanowire Schottky diodes were then fabricated using the oxidized wires and measured using EBIC. Successful oxidation was confirmed by SEM imaging of the near-contact region of the finished devices. The undercut provided by the MMA copolymer layer is used to assist in liftoff after metalization of EBL defined contacts. This also creates an exposed portion of the nanowire that remains uncovered during metal evaporation. Therefore, the

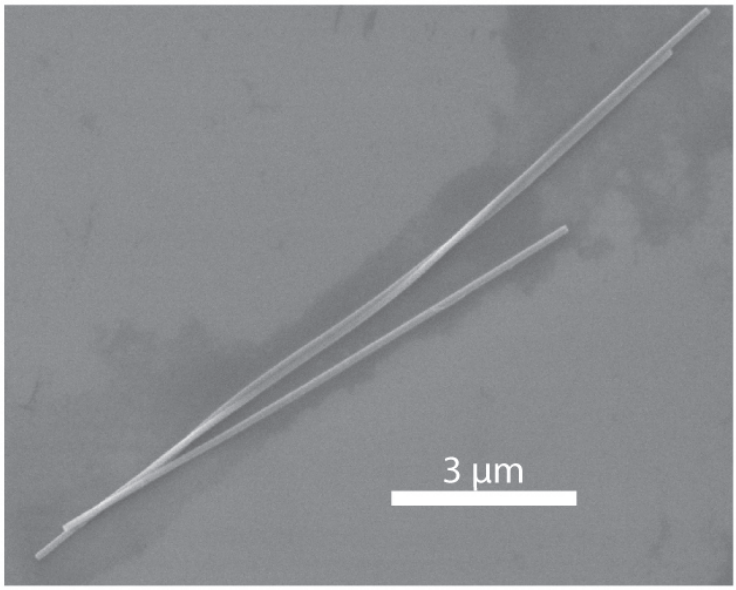

Figure 4.6. SEM image of silicon nanowires after removal of the gold catalysts.

buffered-HF etching of the contact region results in a visible interface where the oxide shell thickness can be measured as shown in Figure 4.7. The imaged nanowire was oxidized for 90 minutes at 650 °C and shows an oxide thickness of ~3.5 nm. After analysis using EBIC, it was found that L_p remained unchanged after oxidation (see Figure 4.8). Previous reports of interface state densities of thermally oxidized silicon nanowires have suggested that the high radius of curvature and non-planar bounding surfaces may limit the minimum achievable density[49,58,59]. The completeness of passivation of the surface states scales with curvature with decreased curvature resulting in a more uniform interface. In addition, strong dependence of interface state density with annealing temperature has been observed in planar silicon[61]. Typically, dry oxidation of silicon is done at temperatures of 900 °C to 1200 °C where it is seen that the surface charge density decreases with increasing annealing temperature. Additional experiments using significantly higher annealing temperatures

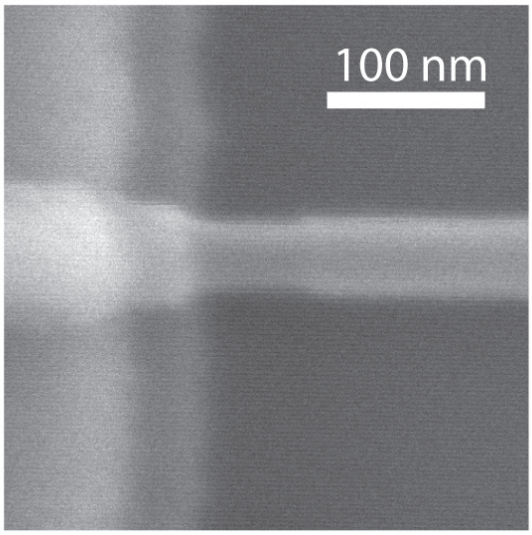

Figure 4.7. SEM image of the near-contact region of a nanowire device fabricated with an oxidized silicon nanowire.

may yield improved interface state densities, however, as mentioned previously, dopant segregation may occur at such high temperatures.

In addition to the inorganic passivation studies, a few attempts at organic passivation were made. There are a number of additional challenges to organic passivation that must be considered. Unlike a thermally grown oxide layer, organic passivation is not necessarily indefinitely stable on the silicon surface. Passivating the nanowires before device fabrication means that the functionalization must remain after at least 24 hours in air and be robust enough to survive all of the fabrication steps including polymer coating and lift-off in acetone. Alternatively, one could try passivating the wires after device fabrication. In this case the processing must not harm the metal or the metal-semiconductor interface. Both of these approaches rule out a simple hydrogen passivation as this is typically not stable for more than a couple of hours and the HF and NH_4F

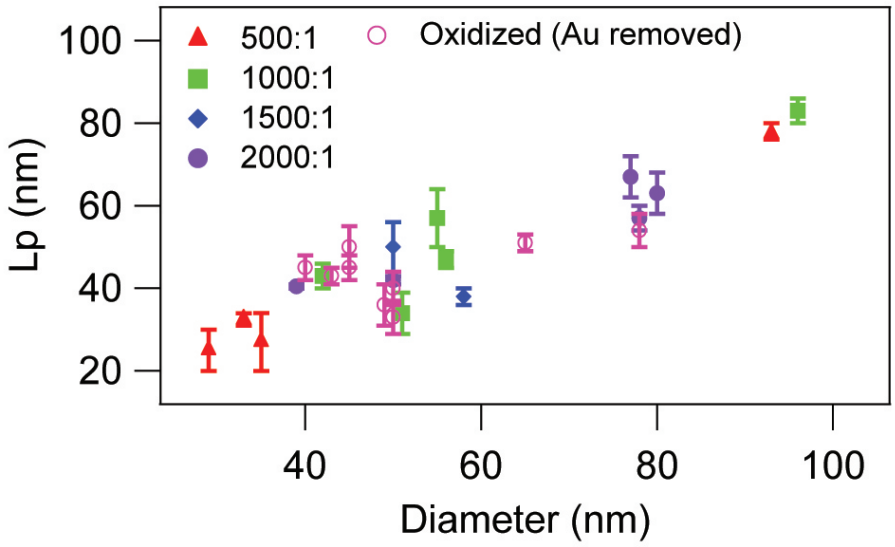

Figure 4.8. Plot of L_p versus diameter repeated from Figure 4.5 with the addition of results obtained from oxidized silicon nanowires. Diameter values for the oxidized wires are the core diameter determined from SEM images of the near-contact region.

solutions were found to damage the contacts. Finally, EBIC involves a high energy focused electron beam which can destabilize the functionalization. Therefore the diffusion length measurements must be done using SPCM instead of EBIC resulting in a significantly reduced resolution. If passivation is successful, of course, the SPCM resolution may not be a limitation.

Functionalization by octadecene ($C_{18}H_{36}$) was carried out in collaboration with Josh Kellar in the Hersam group. Nanowires on the growth substrate were immersed in neat octadecene and irradiated with a UV pen lamp (Spectroline 11SC-1 UV lamp, ~9 mW/cm^2, 254 nm) for 2 hours. The functionalized wires were then used to fabricate nanowire Schottky diodes that were analyzed using SPCM. Unfortunately, this experiment was

conducted before the acquisition of the Witec alpha300 confocal microscope/NSOM system that was used for most of the SPCM studies in this document. The system available at the time suffered from very poor laser focus and an unstable sample stage that significantly affected the resolution of the data. The theoretical resolution of confocal SPCM is approximately 500 nm, so measuring the diffusion length by this method would require a significant reduction in the surface state density and very good measurement conditions. Repeating this experiment using NSOM SPCM on the Witec system would improve the measurement resolution significantly (˜100 nm).

4.5. Ensuring diffusive transport and control experiments

During EBIC measurements, there is a possibility of charging and/or beam damage affecting the results. Therefore a number of control experiments were conducted to confirm that these effects were not altering the measured diffusion lengths. Furthermore a strict criteria for what devices were analyzed was followed. This was necessary due to the fairly large variation in device performance across nanowire Schottky diodes.

Only those devices with low reverse bias saturation current and linear forward bias characteristics above the turn-on voltage were used for EBIC measurements. Current vs. voltage data for devices which had been scanned multiple times were unchanged after exposure to the electron beam (Figure 4.9). Minority carrier diffusion lengths were determined by fitting an exponential to the EBIC signal along the nanowire axis. The decay constants of the exponential fits are the same for different biases applied to the Schottky diode (Figure 4.10), confirming that the transport is diffusive in nature with a negligible drift component. Any slight deviations are indicated by the error bars in Figure

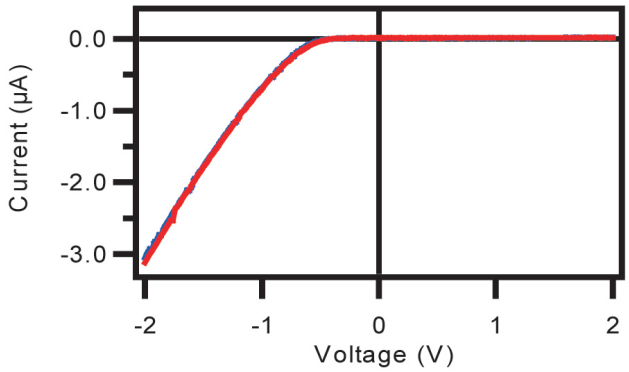

Figure 4.9. Current vs. voltage data from an n-type silicon nanowire Schottky diode before (red) and after (blue) EBIC analysis

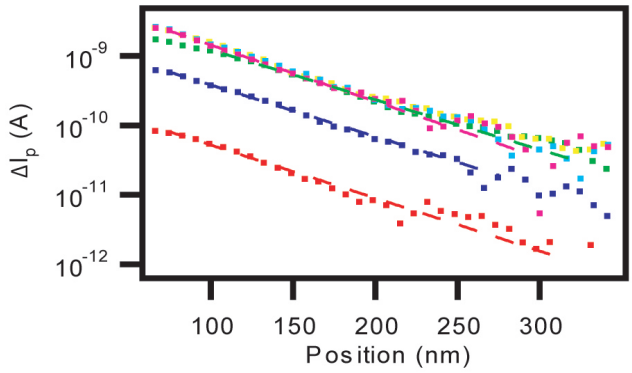

Figure 4.10. EBIC line profiles from an n-type silicon nanowire Schottky diode taken at different reverse bias voltages: Red 0 V, Blue 0.1 V, Green 0.3 V, Yellow 0.5 V, Cyan 1 V, Magenta 1.5 V. The dashed lines are exponential fits to the data (squares)

4.5.

The data presented in Section 4.2 was collected using devices with a silicon dioxide dielectric layer, but control experiments were conducted using a silicon nitride dielectric layer and found no deviation from the measurements on silicon dioxide. When measuring semi-insulating samples, such as these dielectric layers on silicon, it is known that charging can be minimized by the proper choice of accelerating voltage. It was found that at 5 kV,

no visual indication of charging was observed during the measurements. As an additional control to ensure charging was not influencing the measurement, EBIC was performed using an Argon back-pressure in a variable-pressure SEM to neutralize any substrate charging. Again it was found that the measurements in 1 torr of argon were consistent with those made in vacuum.

In EBIC measurements on bulk crystals, the size of the generation volume and the distance of its center from the surface complicate interpretation of the current decay. In our measurements, the finite thickness of the sample limits the lateral spread of the beam because the majority of electrons pass through without scattering. Furthermore, the fact that the sample width is much less than the bulk diffusion length greatly simplifies our analysis, as described in Section 4.1. To further verify that a variation in generation volume was not responsible for the observed diameter scaling of the diffusion length, measurements at different accelerating voltages were made (Figure 4.11); increasing the voltage increases the electron mean free path, which moves the center of the generation volume farther into the sample. No change in the slope of the decay was observed.

4.6. Effect of the MMA undercut on nanowire devices

In section 4.4, the undercut provided by the MMA copolymer layer during EBL was beneficial in providing a means to determine the oxide thickness. In unoxidized nanowire devices the diameter change at this interface is small (< 2 nm), however in some cases there was a significant effect on the nanowire device as indicated by EBIC measurements. The data presented in Figure 4.12c shows a strong peak in the induced current signal at the edge of the undercut region. The location of the undercut is indicated on the SEM

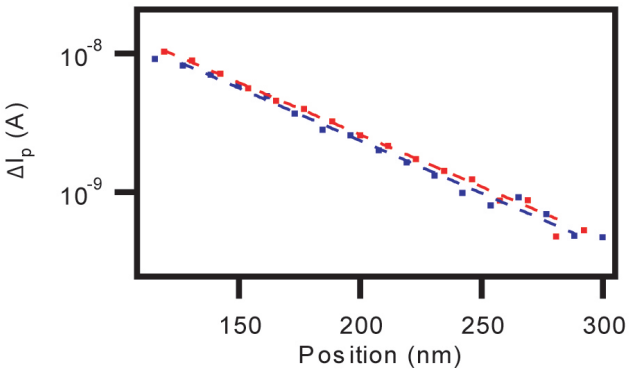

Figure 4.11. EBIC line profiles from an n-type silicon nanowire Schottky diode taken with different electron beam accelerating voltages. The dashed lines are exponential fits to the data (squares). The decay constant of the exponential does not change significantly between 5 kV (red) and 7 kV (blue) beams.

image in Figure 4.12a and is identified by a slight contrast ~130 nm from the metal contact. This effect was not observed on all devices and varied in magnitude significantly between devices. It is likely that this is the result of internal fields created because of the removal of surface doping in the contact region. In this case there will be an abrupt junction at the edge of the undercut that could explain the enhanced signal. The variability in the effect could therefore be explained by variation in the amount of surface doping present. The issue of surface doping in n-type silicon nanowires will be addressed directly in Chapter 5. It should be noted that despite this artifact in the devices, the diffusion length can still be determined by analyzing the exponential decay away from the peak. Far from the junction, it is still expected that the nanowire is field-free. Therefore any induced current is the result of diffusion to the internal field at the junction.

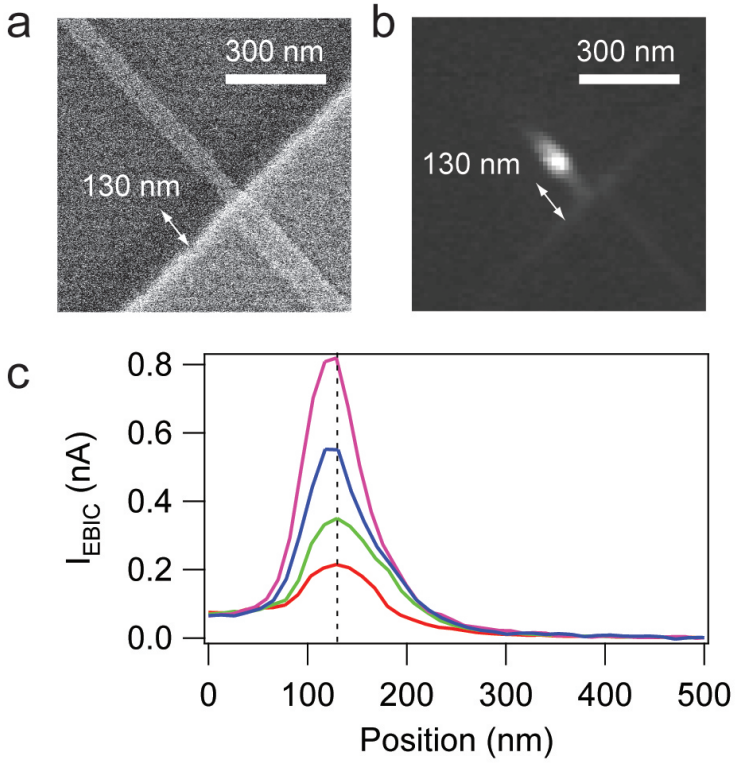

Figure 4.12. Effect of the MMA undercut on EBIC analysis of silicon nanowire Schottky diodes. (a) SEM image showing the extent of the undercut and, (b), the corresponding EBIC image taken at 2 V reverse bias. (c) Line profiles of the EBIC data taken at 0.5 V (red), 1 V (green), 1.5 V (blue), and 2 V (magenta). The vertical dashed line at 130 nm marks the edge of the undercut.

4.7. Summary

The results presented in this chapter advance the quantitative correlation of surface properties and observed electrical properties in nanoscale materials. It was shown that for n-type Si nanowires with diameters less than 100 nm excess carrier recombination is dominated by surface recombination and that $Si-SiO_2$ interface quality may be limited in these wires due to the high surface curvature. Furthermore a quantitative estimate of the

interface state density was made; similar analysis on modified nanowires could be used to quantify improvements to the interface. Additionally, the work shows the potential for scanning probe techniques to directly probe material properties in semiconductor nanowires that are integrated into nanoscale devices.

Since the original publication of this work[42], similar analysis on large diameter Si nanowires (1 to 2 μm) was published showing diffusion lengths of 1 to 2 μm[48] consistent with the diameter scaling presented here. Recently optical measurements of excess carrier lifetimes in Ge nanowires also show very short lifetimes that are surface dominated and diameter dependent[83] further supporting this work.

CHAPTER 5

Non-uniform nanowire doping profiles revealed by scanning photocurrent microscopy

The future of semiconductor nanowires as building blocks for high-performance nanoscale devices is promising. However, it remains an important challenge to synthesize materials with sufficient control over composition and doping to compete with existing commercial devices. For example, the performance of existing CMOS technology depends critically on the ability to control the location of dopants to create abrupt homojunctions in Si. Such junctions have been realized in Si nanowires synthesized using the VLS growth mechanism by *in-situ* doping[10,29], but unintentional surface doping caused by vapor-solid (VS) deposition on the sides of the nanowires[47] during growth can complicate the formation of strictly axial homojunctions. Evidence of surface doping has been seen in phosphorous-doped Ge nanowires by electrical characterization[47] and atom probe tomography[40,41], and in boron-doped Si nanowires by Raman spectroscopy[57]. In each of these cases, the nanowires were highly tapered, which is indicative of significant VS deposition during synthesis. It is possible in principle to eliminate surface doping by eliminating VS deposition[31], but the results presented here show that surface doping can occur in VLS nanowires even in the absence of measurable taper.

In this chapter the use of SPCM to detect axial doping profiles in phosphorous-doped n-type silicon nanowires will be presented. A nonuniform photocurrent response along

the length of the devices indicates a nonuniform electric field that can be attributed to a resistivity gradient. Wet chemical etching of the nanowire surface within the device channel leads to a uniform electric field consistent with uniform doping within the nanowire after removal of a surface doping layer. Furthermore, the use of four-terminal device geometries has facilitated the determination of quantitative potential profiles from SPCM profiles for the first time. A simple semi-quantitative model of the SPCM signal is then used to derive effective electron concentrations before and after etching. These results further the understanding of impurity incorporation during VLS nanowire growth and have implications for the interpretation and design of nanowire devices.

5.1. Supporting calculations for SPCM

Before describing the experimental application of SPCM analysis to nanowire devices, some calculations covering the basic assumptions in the SPCM interpretation will be presented. First, the expected excess carrier concentration will be calculated in order to confirm the low-injection condition. This ensures that injected carriers may be used to probe, but not perturb, the local potential. Next, the excess carrier distribution will be calculated using the ambipolar transport equations. Using an effective carrier lifetime estimated from the measured minority carrier diffusion length from Chapter 4, it is shown that the excess hole population is largely confined to the excitation region. A model for the expected SPCM signal is presented based on a simple series resistance approximation.

5.1.1. Carrier injection level versus laser power

The interpretation of SPCM results is greatly simplified provided the low-injection condition is met. Low-injection is defined as $\Delta p << n_0$ for an n-type semiconductor and ensures that the population of excited carriers is sufficiently low that it does not significantly perturb the potential of the device. The following calculation gives an estimate of the injection level which is found to be significantly lower than the expected wire doping levels for the range of laser powers used in this study.

Given a laser spot size of diameter w and nanowire of radius r, the number of photons incident on the wire is given by

$$\text{Incident Photons} = \Phi(2\text{rw}) \tag{5.1}$$

where

$$\Phi = \frac{\text{I}_0/\text{h}\nu}{\text{A}_{\text{spot}}} \tag{5.2}$$

I_0 is the incident laser power, and $h\nu$ is the energy per photon. A_{spot} is the area of the laser spot and is equal to $\pi(w/2)^2$. This assumes a top-hat beam profile with uniform intensity within a circular spot. In reality the beam is Gaussian and therefore does not have a uniform intensity profile. This results in an underestimation of the peak intensity by roughly a factor of two. As will be seen below, doubling the laser intensity still results in low-injection. For a Gaussian beam, the spot size is given by: $w = FWHM/1.18 \times 2$. Approximating the nanowire to a rectangular prism of cross section $2r \times 2r$, the number

of absorbed photons is given by

$$\text{Absorbed Photons} = \text{Incident Photons} \times (1 - \mathrm{e}^{-2\mathrm{r}\alpha}) \tag{5.3}$$

where α is the absorption coefficient at the excitation wavelength. Assuming a rectangular cross-section in this step results in an overestimation of the number of absorbed photons. Since the calculation is meant to confirm low-injection, an overestimation here is only significant if the excess carrier concentration is found to be in the high-injection regime. Assuming that each absorbed photon creates an electron-hole pair, the generation rate is given by

$$\mathrm{g} = \frac{\text{Absorbed Photons}}{\text{Volume}} \tag{5.4}$$

and

$$\text{Volume} = \mathrm{w} \times \pi \mathrm{r}^2 \tag{5.5}$$

Finally, the excess carrier population in the illuminated region, δp, is equal to $g\tau_p$ where τ_p is the carrier lifetime. Figure 5.1 shows the calculated excess hole concentration versus laser power for a 50 nm silicon nanowire. In this case, τ_p was calculated from the measured diffusion length (see Chapter 4) using the Einstein relation: $\tau_p = L^2 q/\mu_p kT$. Using the bulk mobility for minority holes[80] (~150 $\mathrm{cm}^2/\mathrm{Vs}$ for n=1×10^{18} cm^{-3}), the effective lifetime for a 50 nm silicon nanowire is approximately 3 ps. It should be noted that the Einstein relation is only valid for nondegenerate semiconductors. Expected doping levels in the wires studied range from 1×10^{18} cm^{-3} to 1×10^{20} cm^{-3} which easily fall

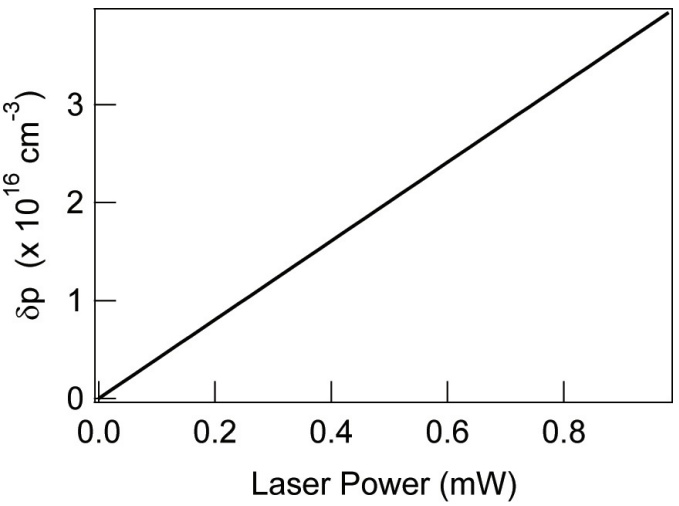

Figure 5.1. Excess hole concentration versus laser power for a 50 nm silicon nanowire.

into the degenerate doping regime. Based on a report from Trajkovic et al.[84], using the nondegenerate Einstein relationship for silicon doped at these levels will result in an underestimation of the minority carrier lifetime by a factor of 1.4 (1×10^{18} cm^{-3}) to 10 (1×10^{20} cm^{-3}). At the laser powers used for this study (˜10 μW to ˜45 μW), even a factor of ten increase in the excess carrier concentration will still be almost four orders of magnitude lower than the majority carrier concentration. This calculation indicates that the measurements presented in this work were conducted under low injection. This is confirmed experimentally in section 5.1.4.

5.1.2. Excess carrier distribution

This section details the application of the ambipolar transport equation to calculate simulated excess carrier concentration profiles in a one-dimensional extrinsic semiconductor with local excitation in low-injection. The purpose of these calculations is to demonstrate the extent of excess carrier drift as a function of electric field. It is shown that in silicon

nanowires the short diffusion length will confine excess carriers to the excitation region except in exceptionally high electric fields. This has significant implications in the interpretation of the photocurrent signal. The localized influence of excess carriers allows the photocurrent signal to be interpreted as a local change in wire resistance rather than a more complicated consideration of continuity and gain mechanisms.

It is possible to solve the problem analytically following a number of simplifications. First, it is assumed that the electric field in the device is constant. Our measurements show that this is clearly not the case; however including a functional form for the electric field significantly complicates the series of differential equations. Instead, the solution for a uniform field will be presented for a range of electric fields. While this does not quantitatively represent the expected profiles in real nanowire devices, it still may be used to estimate relevant length scales. The second assumption is that there is no field in the generation region. For this calculation, the area of interest is outside of the excitation region, and this assumption should not significantly affect the excess hole distribution outside of the excitation region.

The behavior of nonequilibrium excess carriers in semiconductors can be described by the ambipolar transport equation. Upon injection of a nonequilibrium population of electrons and holes in the semiconductor, the carriers will diffuse due to the introduced concentration gradient and will drift in any electric fields present. The ambipolar transport equation takes into account the internal field created when the excess electrons and holes are separated that attracts the carriers back together. In the limits of extrinsic doping and low carrier injection the transport parameters of both carrier types reduce to the

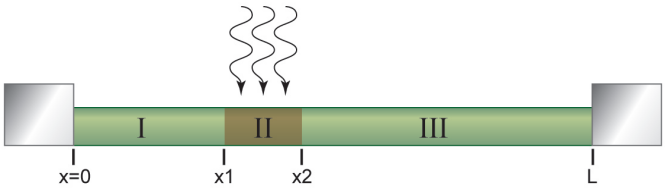

Figure 5.2. Diagram of a nanowire device showing regions used for excess carrier distribution calculations.

minority carrier values and the one-dimensional ambipolar transport equation becomes

$$\mathrm{D_p}\frac{\partial^2(\delta \mathrm{p})}{\delta \mathrm{x}^2} - \mu_\mathrm{p}\mathrm{E}\frac{\partial(\delta \mathrm{p})}{\delta \mathrm{x}} + \mathrm{g} - \frac{\delta \mathrm{p}}{\tau_\mathrm{p}} = \frac{\partial(\delta \mathrm{p})}{\partial \mathrm{t}}$$

where μ_p is the hole mobility, E is the electric field, g is the carrier generation rate, and δp is the excess hole concentration. We must now consider the solution to this equation in three different regions of the nanowire. These regions are indicated on Figure 5.2 and are as follows. Region II is the excitation region of the device. Here there is direct excitation of excess carriers from the excitation source. The extent of this region is from $x1$ to $x2$ where $x2-x1 = w$ and w is the excitation spot size. Regions I and III bound Region II and do not see direct excitation of excess carriers. However in this region there is an electric field and we will expect drift and diffusion of excess carriers from Region II to extend into these two regions. Based on these definitions we can make a number of simplifications to the transport equations. The period of oscillation for excitation modulation during SPCM measurements was on the order of milliseconds. This is sufficiently slow compared to generation and recombination processes for the measurement to be considered steady-state. Therefore, $\partial(\delta p)/\partial t = 0$ for all three regions. Outside of Region II, there is no generation, so for Regions I and III, $g = 0$. Finally, as mentioned earlier, the electric field

in Region II is assumed to be zero. Using these assumptions the equations become:

$$\begin{aligned}
\text{Region I} \quad &: \quad D_p \frac{\partial^2(\delta p)}{\delta x^2} - \mu_p E \frac{\partial(\delta p)}{\delta x} - \frac{\delta p}{\tau_p} = 0 \\
\text{Region II} \quad &: \quad g - \frac{\delta p}{\tau_p} = 0 \\
\text{Region III} \quad &: \quad D_p \frac{\partial^2(\delta p)}{\delta x^2} - \mu_p E \frac{\partial(\delta p)}{\delta x} - \frac{\delta p}{\tau_p} = 0
\end{aligned}$$

Dividing Regions I and III by D_p and using the Einstein relation, it becomes:

$$\begin{aligned}
\text{Region I} \quad &: \quad \frac{\partial^2(\delta p)}{\delta x^2} - \frac{e}{kT} E \frac{\partial(\delta p)}{\delta x} - \frac{\delta p}{L_p^2} = 0 \\
\text{Region II} \quad &: \quad g - \frac{\delta p}{\tau_p} = 0 \\
\text{Region III} \quad &: \quad \frac{\partial^2(\delta p)}{\delta x^2} - \frac{e}{kT} E \frac{\partial(\delta p)}{\delta x} - \frac{\delta p}{L_p^2} = 0
\end{aligned}$$

As was mentioned above, the Einstein relation is only valid for nondegenerately doped semiconductors. Degenerate doping in silicon will result in a constant factor of 1.4 to 10 to the coefficient of the second term depending on the doping level. In each of these regions, the equations can be solved for δp to give:

$$\begin{aligned}
\text{Region I} \quad &: \quad \delta p_I = C_1 e^{r_1 x} + C_2 e^{r_2 x} \\
\text{Region II} \quad &: \quad \delta p_{II} = g\tau_p \\
\text{Region III} \quad &: \quad \delta p_{III} = C_3 e^{r_1 x} + C_4 e^{r_2 x} = 0
\end{aligned}$$

where

$$\mathrm{r_{1,2}} = \frac{\frac{\mathrm{e}}{\mathrm{kT}}\mathrm{E} \pm \sqrt{(-\frac{\mathrm{e}}{\mathrm{kT}}\mathrm{E})^2 + 4/\mathrm{L_p^2}}}{2}$$

and C_{1-4} are constants. These constants can be determined by setting up the following boundary conditions. The carrier concentration must be continuous, so $\delta p_I(x1) = \delta p_{II}(x1) = g\tau_p$ and $\delta p_{II}(x2) = \delta p_{III}(x1) = g\tau_p$. Furthermore, at the contacts it is expected that the excess carriers will be swept out of the device quickly because of the large field at the metal-semiconductor junction. This implies that $\delta p_I(0) = 0$ and $\delta p_{III}(L) = 0$. These boundary conditions give

$$\begin{aligned} \mathrm{C}_1 &= \frac{g\tau_p}{e^{r_1 x1} - e^{r_2 x1}} \\ \mathrm{C}_2 &= -\frac{g\tau_p}{e^{r_1 x1} - e^{r_2 x1}} \\ \mathrm{C}_3 &= -\frac{g\tau_p e^{(r_2 - r_1)L}}{e^{r_2 x2} - e^{r_2 L + r_1(x2-L)}} \\ \mathrm{C}_4 &= \frac{g\tau_p}{e^{r_2 x2} - e^{r_2 L + r_1(x2-L)}} \end{aligned}$$

With the constants known, the excess hole population can be calculated as a function of position. The calculation was made for a 50 nm nanowire with a 10 μm channel length. As before, the minority carrier lifetime was calculated from the minority carrier diffusion length measured by EBIC. The measured valued for L_p, ~50 nm, was used (see Chapter 4) and a bulk mobility was assumed. The generation rate was calculated as described in the previous section using 42 μW for the laser power. The results, presented in Figure 5.3, show that even for large electric fields (10,000 V/cm) the excess holes are primarily localized to the excitation region. On a semi log scale (Figure 5.3b) it is clear that the electric field does shift the excess carrier distribution, but not significantly. The maximum field plotted in Figure 4 is 10,000 V/cm which for the 10 μm channel would correspond

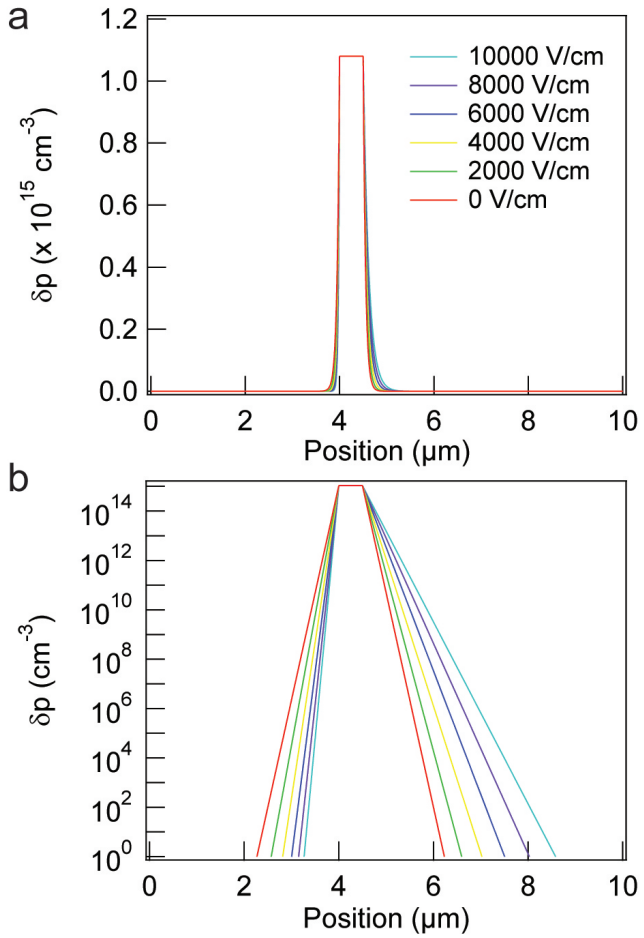

Figure 5.3. Calculated excess hole distributions for electric fields from 0 V/cm to 10,000 V/cm. Data is plotted on a linear scale, (a), and a semilogarithmic scale, (b).

to a 10 V applied bias. In Chapter 5, quantitative potential profiles were determined for long-channel nanowire devices with applied biases of -5 to 5 V. The maximum field observed in these devices is approximately 8,000 V/cm.

5.1.3. Estimated photocurrent

In the previous two sections, it was established that during the SPCM measurements of nanowire devices presented in this study, the excitation is in the low-injection regime and the excess carrier population is localized to the excitation region. With this in mind, it is possible to estimate the expected photocurrent for a uniform device. In this case, locally increased carrier concentrations will result in a decreased local resistance. For a uniform nanowire device with ohmic contacts, the device current is determined by the wire resistance according to Ohm's Law, I=V/R. When the resistance of one segment of the wire is decreased, the total resistance, R, decreases and the current will increase. The change in current will be given by

$$\Delta I = I_2 - I_1 = \frac{V_2}{R_2} - \frac{V_1}{R_1} = \frac{V(R_1 - R_2)}{R_1 R_2}$$

If we assume that $\Delta R << R$ (valid for low injection), then this becomes

$$\Delta I = -\frac{V}{R^2}\Delta R \tag{5.6}$$

The change in resistance, ΔR, is equal to the change in resistance of the illuminated segment given by

$$\Delta R = \frac{\Delta \rho w}{A} \tag{5.7}$$

where w is the laser spot size and A is the cross-sectional area of the nanowire. The change in resistivity is given by

$$\Delta\rho = \rho_2 - \rho_1 = \frac{1}{\sigma_2} - \frac{1}{\sigma_1} = \frac{\sigma_1 - \sigma_2}{\sigma_1\sigma_2} \tag{5.8}$$

The conductivities, σ_1 and σ_2", are given by

$$\begin{aligned} \sigma_1 &= \frac{1}{\rho_1} = \frac{L}{RA} \\ \sigma_2 &= \sigma_1 + \Delta\sigma = \frac{L}{RA} + e\mu_h\Delta p \end{aligned} \tag{5.9}$$

where L is the channel length. It is assumed that the carrier mobility is unchanged. Since the measurement is conducted in low-injection, changes in mobility should be negligible. Given that the excess carrier concentration can be calculated as described in the earlier sections, it is then possible to solve for the change in current, or photocurrent, in Equation 5.6. Substituting Equations 5.9 into Equation 5.8, the change in resistance becomes

$$\Delta\mathrm{R} = \frac{-\mathrm{e}\mu_\mathrm{h}\mathrm{w}\Delta\mathrm{p}}{\frac{\mathrm{L}}{\mathrm{R}}(\frac{\mathrm{L}}{\mathrm{RA}} + \mathrm{e}\mu_\mathrm{h}\Delta\mathrm{p})} \tag{5.10}$$

Using the calculated value for Δp at 42 μW (~1×10^{15} cm^{-3})and assuming bulk-like mobility[85], Equation 5.6 gives the expected photocurrent as a function of the applied bias as shown in Figure 5.4. For this calculation, parameters were chosen to match the devices presented later in this chapter. The red plot was calculated using the following parameters: R=550 kΩ, L=13 μm, w=500 nm, A=7.85×10^{-11} cm^2, and $\mu_h = 100cm^2/Vs$. The blue plot was calculated using the following parameters: R=2 MΩ, L=10 μm, w=500

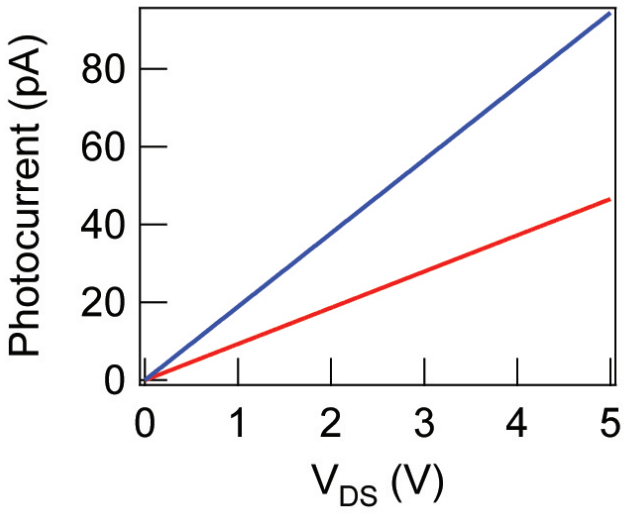

Figure 5.4. Calculated photocurrent versus applied bias for uniform silicon nanowire devices. Parameters for the calculations for each curve are as follows. Red: R=550 kΩ, L=13 μm, w=500 nm, A=7.85×10^{-11} cm^2, and $\mu_h = 100 cm^2/Vs$. Blue: R=2 MΩ, L=10 μm, w=500 nm, A=7.85×10^{-11} cm^2, and $\mu_h = 120 cm^2/Vs$

nm, A=7.85×10^{-11} cm^2, and $\mu_h = 120 cm^2/Vs$. These plots show that expected photocurrent magnitudes are on the order of tens of pA. As will be seen in the forthcoming analysis, this prediction is consistently lower than the observed signal, but within a factor of ten. In part this may be due to the underestimated excess carrier lifetime resulting from the improper application of the nondegenerate Einstein relation. As was mentioned previously, the Einstein relation underestimates the carrier lifetime by a factor of 1.4 for n=1×10^{18} cm^{-3} to 10 for n=1×10^{20} cm^{-3}.

The above calculation assumes a uniform nanowire with $L_p << w$. Therefore the analysis can be reduced to a simple treatment of a change in conductivity due to an increase in drift current in that region. However it is necessary to point out that if L_p is significantly extended or if w is significantly decreased, the treatment must then account

for the distribution of excess carriers arising from both drift and diffusion outside of the generation region.

5.1.4. Four-terminal n-Si nanowire device fabrication and characterization

VLS-grown n-type Si nanowires doped with phosphorous were used to fabricate long channel nanowire devices with low contact resistance. Nanowires were synthesized via low-pressure CVD with solution-deposited mono disperse 50 nm gold catalyst particles. The ratio of precursor gases in the reactor during synthesis was 500:1 SiH_4:PH_3 to give heavily doped n-type nanowires. Detailed growth conditions can be found in Appendix C. Devices consisted of four electrodes on a single nanowire with a long ($> 10\ \mu m$) middle channel. Details of device fabrication can be found in Chapter 3. The four-probe device geometry allows for accurate determination of the series resistance of the contacts (see Section 3.2.1), while the long middle channel facilitates the study of variations in the local photocurrent response over relatively long length scales. Two-terminal I-V characteristics were linear, and four-terminal measurements indicated that contact resistances were typically less than 5% of the total two-terminal device resistance confirming that the nanowire is the dominant resistance in the devices under study.

5.2. Evidence of surface doping profiles

SPCM measurements were performed using a confocal microscope to focus above-bandgap (532 nm) illumination onto a sample mounted on a piezoelectric scanning stage. Additional information about the details of the measurement are given in Chapter 3. Figure 5.5 shows the SPCM analysis of a typical n-Si nanowire device. Figures 5.5a and

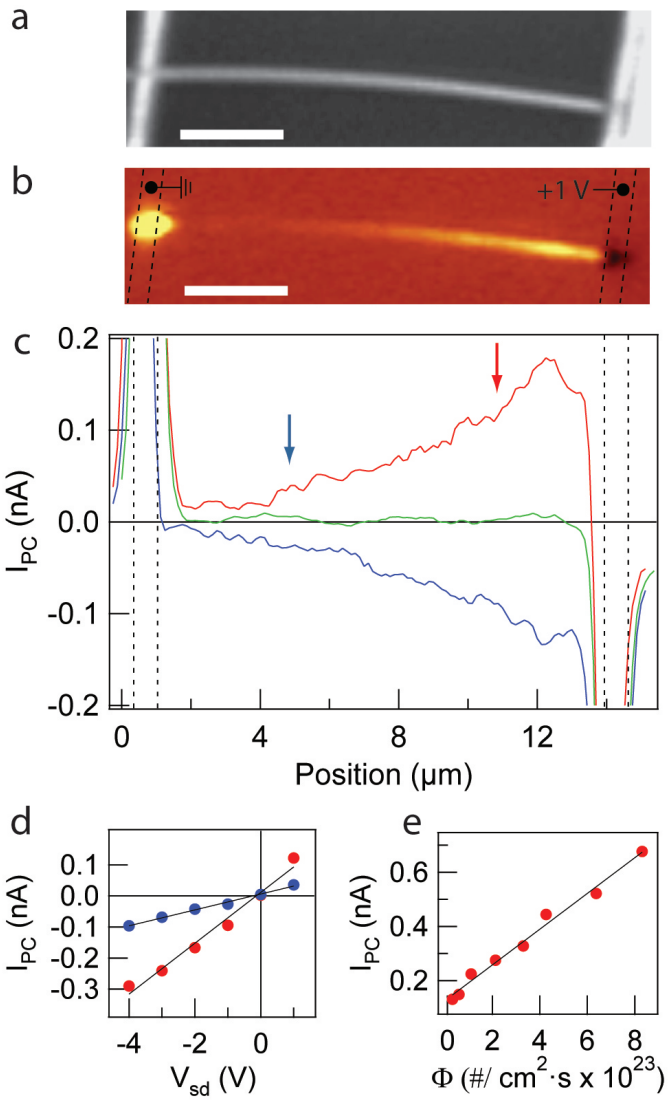

Figure 5.5. SPCM analysis of an n-Si nanowire device. (a) Reflection image of the nanowire device and corresponding SPCM image, (b), taken with 1 V bias applied to the right contact. (c) Line profiles taken along the device channel for SPCM scans at 1 V (red), 0 V (green), and -1 V (blue). Vertical dashed lines indicate the location of the metal contacts. (d) Local photocurrent response versus applied bias taken at two points along the channel indicated by the arrows in 'c'. (e) Local photocurrent response versus photon flux from the region marked by the red arrow in 'c'. Scale bars are 3 μm.

5.5b were obtained in parallel with Figure 5.5a being the reflection signal and Figure 5.5b showing the photocurrent map. Bright (dark) contrast in the photocurrent image corresponds to positive (negative) photocurrent. The nature of the response at the contacts has been discussed previously[65,67] and is not the focus of this study (details of those findings are summarized in Chapter 2). Instead, the local photocurrent in the device channel is analyzed to provide insights into inhomogeneities in the electrostatic potential that arise from the nanowire material, rather than the device geometry. Local illumination of the nanowire creates excess electron-hole pairs by interband excitation. In the presence of an electric field, the excess free carriers drift at a rate proportional to the magnitude of the electric field, producing a current. This photocurrent $I_{ph}(x)$ will be directly proportional to the local electric field $E(x)$ provided that $\Delta p << n_0$ (the low-injection condition) and that minority carrier drift-diffusion lengths are much shorter than the channel length. Measured diffusion lengths for these wires are on the order of the wire diameter[42], and, in addition to the injection-level calculation in section 5.1, the low-injection condition was confirmed by a linear increase in photoconductivity with laser power (Figure 5.5e). Line profiles of the photocurrent in the channel region at applied biases of 1 V, 0 V, and -1 V are shown in Figure 5.5c. The signal varies linearly with the applied bias (Figure 5.5d) and increases monotonically from left to right. Because $I_{ph}(x) \propto E(x)$, it follows that the electric field is non-uniform reaching a maximum at the right side of the device. The shape of the photocurrent profile does not change even if the biasing electrode is switched, indicating a negligible influence of the grounded back gate electrode. Therefore, the observed field gradient is due to intrinsic variations within the nanowire itself rather than a

consequence of its integration into a device. Next the possible sources of the field gradient are discussed.

From Ohm's law it is given that the electric field in the nanowire is proportional to the resistivity:

$$\mathrm{J(x)} = \sigma\mathrm{(x)E(x)} \rightarrow \mathrm{E(x)} = \frac{\rho\mathrm{(x)}}{\mathrm{A(x)}}\mathrm{I_{DC}} \tag{5.11}$$

where I_{DC} is the DC current through the device, ρ is the resistivity and A is the cross-sectional area of the nanowire. The photocurrent will therefore be greatest in the region where the differential resistance, ρ/A, is highest. For the nanowire shown in Figure 5.5, and all other nanowires examined in this study, the region of the nanowire closest to the catalyst tip showed the largest photocurrent response. This indicates that either the nanowire area or conductivity (ρ^{-1}) is decreasing towards the tip of the nanowire. Atomic force microscopy (AFM) measurements of the nanowire in Figure 5.5 show no measurable taper over the 13 μm channel length. Since the nanowire cross-section is constant, the inhomogeneous electric field results from a resistivity gradient. A resistivity gradient may arise from a variation in dopant or unintentional impurity concentration along the nanowire. In VLS grown nanowires, the possibility of catalyst contamination should be considered. Au is known to compensate majority carriers in Si and could therefore increase the resistivity of the material in areas of increased Au concentration[43]. We have recently determined an upper-bound of on the concentration of Au atoms in similar nanowires ($5 \times 10^{17}\ cm^{-3}$)[42]. The magnitude of variation in carrier concentration described below is too large to be accounted for by Au contamination. Instead, we propose that a resistivity gradient exists along the length of the wire due to the continuous surface incorporation of

phosphorous atoms during growth. The partial pressure of PH_3 was held constant during growth, so one expects uniform doping in the interior of the nanowire. PH_3 decomposition on the nanowire surface, however, could lead to increased doping and lower resistivities towards the base of the nanowire. The resulting resistivity gradient would produce a non-uniform photocurrent response as seen in our SPCM measurements. If the surface doping were eliminated, the resistivity gradient would also be eliminated.

5.3. Removal of surface doping profiles by surface etching

To test the hypothesis that the resistivity gradient can be removed by etching the surface doping, sequential SPCM studies were conducted before and after surface etching of a nanowire device. A thick layer of PMMA resist was spin-coated on the devices to protect the metal contacts, and windows were opened in the device channel using electron-beam lithography followed by a short oxygen plasma clean. The native oxide was removed using a 2-second buffered HF etch, and a few nanometers of the Si surface were subsequently removed by a 20-second NH_4F etch. A schematic of the pre and post-etch device is shown in Figure 5.6a. AFM measurements indicated that 2 to 4 nm was etched from the surface of the wires, corresponding to a diameter reduction of 4 to 8 nm (Figure 5.6b). Approximately 1 nm of the 200 nm Si_3N_4 dielectric layer was also removed by the etch, which did not significantly impact the properties of the dielectric.

Electrical characterization of the etched devices confirmed that a small amount of surface etching resulted in a disproportionate change in wire resistance as expected for wires with surface doping. Figures 5.7a and 5.7b show the four-probe I-V data for devices with 2 nm and 4 nm of surface etching, respectively. The contact resistance did not

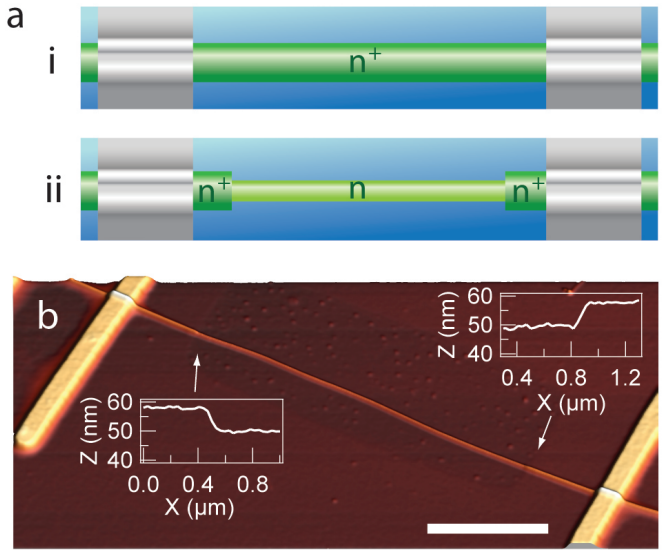

Figure 5.6. Surface etching of n-Si nanowire devices. (a) Top-down schematic of an etched device before, (i), and after, (ii), surface etching. (b) AFM image of a device after surface etching. Line profiles show the change in height at each side of the etched region. The scale bar is 3 μm.

change significantly. After 2 nm of etching, the wire resistance increased by a factor of three whereas the cross-sectional area was reduced by only 20%. The disproportionate increase in resistance indicates that the resistivity of the remaining material is higher than the material that was removed, consistent with enhanced doping at the surface. We note that the very small amount of material removed means that an equivalent advance of a surface depletion layer cannot by itself account for the change in resistivity. Wires with a deeper surface etch of 2.5 to 4 nm showed more dramatic changes in resistance (Figure 5.7b) which can be attributed in part to the creation of potential barriers at the n^+-n junctions at the edge of the etch window. This will be discussed in detail in Chapte 6. In both cases, current versus gate voltage measurements indicate that the devices remain n-type and show increased transconductance (Figure 5.7e). Removal of the heavily doped

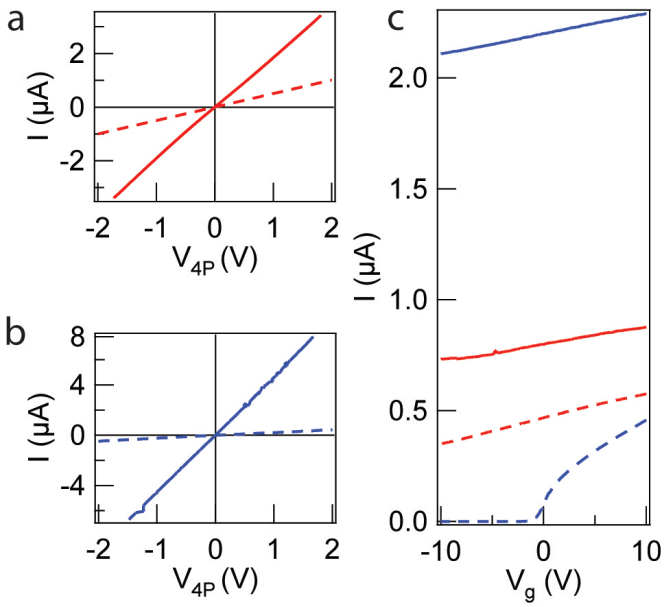

Figure 5.7. Change of nanowire conductivity with surface etching. (a),(b) Four-probe I-V data for devices before (solid line) and after (dashed line) etching of 2 nm and 4 nm, respectively. (c) Current versus gate voltage data for the devices in 'c' and 'd' showing n-type character and enhanced transconductance after etching.

surface layer eliminates a high density of surface charge that would otherwise screen external fields from the back gate. In addition, changes in mobility may accompany the changes in carrier concentration, though the relative contributions of electron-electron and impurity scattering have not been determined.

Etched nanowire devices exhibit a uniform SPCM response in the etched region confirming removal of the doping gradient. Figure 5.8 shows the SPCM analysis following a 2 nm surface etch of the device presented in Figure 5.5. The photocurrent signal is confined to the etched region of the channel (Figure 5.8b) which can be identified by the slight contrast observed in the reflection image of Figure 5.8a. Line profiles of the SPCM signal reveal a uniform response over 10 μm in the etched region confirming that the resistivity

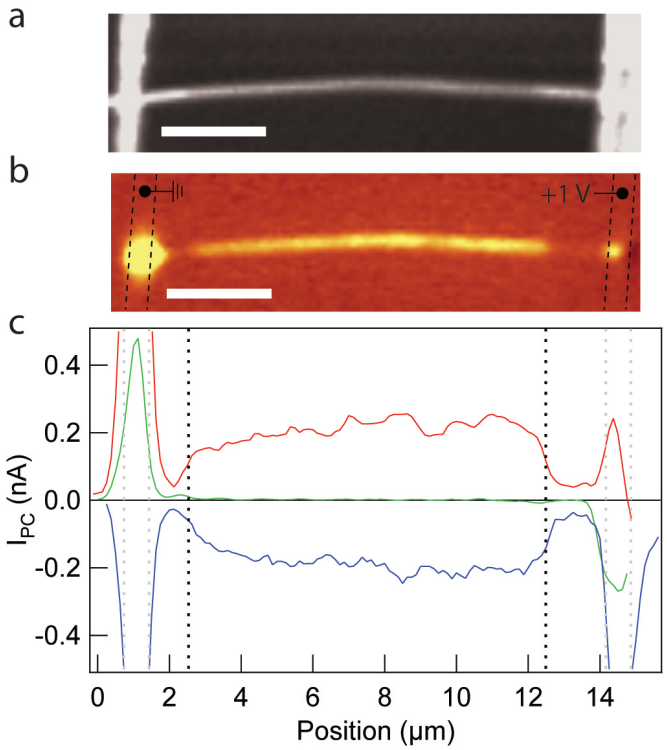

Figure 5.8. SPCM analysis of an n-Si nanowire device with etched channel. (a) Reflection image of the nanowire device and corresponding SPCM image, (b), taken with 1 V bias applied to the right contact. (c) Line profiles taken along the device channel for SPCM scans at 1 V (red), 0 V (green), and -1 V (blue). Vertical dashed black lines mark the extent of the etched region and the location of the metal contacts are indicated by the dashed gray lines. Scale bars are 3 μm.

gradient has been reduced by the surface etching (Figure 5.8c). Further analysis allows for the quantitative determination of one-dimensional potential profiles within the device.

5.4. Quantitative determination of potential profiles and effective electron concentration

Quantitative analysis of the SPCM profiles along the nanowire axis enables us to determine the electrostatic potential and effective carrier concentrations versus position

for both the etched and unetched wires. The photocurrent is proportional to the local field:

$$\mathrm{I_{ph}(x) = \alpha E(x) = -\alpha \frac{dV(x)}{dx}} \tag{5.12}$$

where α is an unknown constant. In this section, α is determined empirically as described below, however it should be noted that this constant is related to the excess minority carrier distribution in the material. Therefore, treating this value as a constant assumes that the excess hole concentration in the generation region, $g\tau_p$, does not vary when the excitation source is moved along the nanowire axis. Also variations in the drift and diffusion of excess carriers outside of the generation region are neglected. This is supported by the discussion in Section 5.1.3.

The empirical analysis is restricted to the region away from the contacts because the contact response has a different functional form. Schematics detailing the procedure for analysis of the potential profiles in a nanowire device are given in Figure 5.9. Integrating over the length of the analyzed region, we find that

$$\int_{x1}^{x2} \mathrm{I_{ph}(x)dx} = -\alpha \int_{V_1}^{V_2} \frac{dV(x)}{dx} dx = -\alpha(V_2 - V_1) \tag{5.13}$$

where $V_2 - V_1$ is the potential drop in the analyzed portion of the nanowire (Figure 5.9). The total potential drop in the nanowire is given by $IR_{NW} = I(R_I + R_{II} + R_{III})$, where R_{NW} is the total nanowire resistance known from four-terminal measurements, and R_I, R_{II}, and R_{III} are the resistances of each segment of the nanowire channel indicated in Figure 5.9a and $V_2 - V_1 = IR_{II}$. The potential drops in each segment of the wire are determined by integrating the photocurrent signal to produce a pseudo potential profile

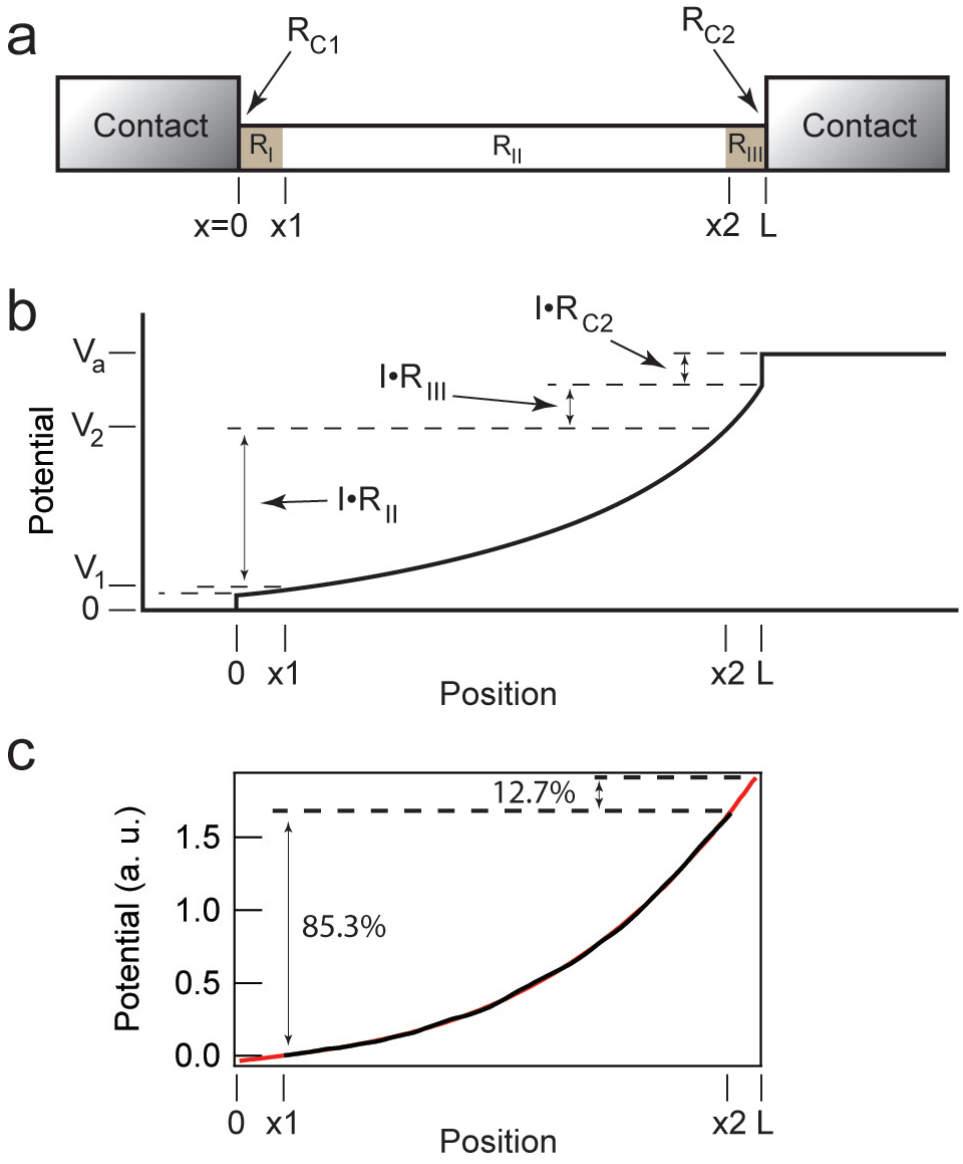

Figure 5.9. Quantitative analysis of nanowire potential profiles. (a) Diagram of a two-terminal nanowire device. Shaded segments of the device channel represent the unanalyzed portion. (b) Expected potential profile of the device in 'a' accounting for contact resistance and a nonuniform resistivity. (c) Pseudo potential profile obtained from SPCM (black) and extrapolated polynomial fit (red) which extends to the edges of the device channel. Relative potential drops of each region are indicated in the plot.

(Figure 5.9c), fitting a polynomial to the photocurrent profile, and extrapolating the fit into the regions in which the contact response dominates. From the extrapolated fit the relative potential drops in each segment of the nanowire channel can be determined. Based on the fit, $V_2 - V_1 = 0.875V_{NW}$, and from the four terminal measurements, $V_{NW} = 0.97V_a$ as the contact resistance is 3% of the total resistance. The applied bias, V_a, is known enabling determination of α from Equation 5.12. The field and potential at an arbitrary position can then be determined as $E(x) = I_{ph}(x)/\alpha$.

Quantitative potential profiles for a device before and after surface etching are given in Figure 5.10. Before etching the profiles are nonlinear, increase in slope toward the nanowire tip, and are unchanged when scaled by the applied bias. After etching the potential profiles are linear within the etched region and relatively flat in the unetched portion of the device for moderate biases. At large positive biases, the profiles become nonlinear with increasing slope toward the biased electrode. As discussed previously, the removal of surface doping reduces the available charge to screen external fields from the back gate. At high positive bias the grounded gate electrode is at a negative potential with respect to the biased electrode and at an equipotential with the grounded electrode. The gate therefore induces depletion on the biased side of the device, leading to a nonuniform carrier concentration and potential profiles that increase in slope toward the biased electrode. It is important to note that the profiles were plotted after setting $V_1 = 0$. In fact, $V_1 = I(R_{C1} + R_I)$, but from four-probe analysis we can establish an upper bound on these resistances indicating that $V_1 < 0.035V_a$. Potential differences between positions within the analyzed region are not affected by this offset.

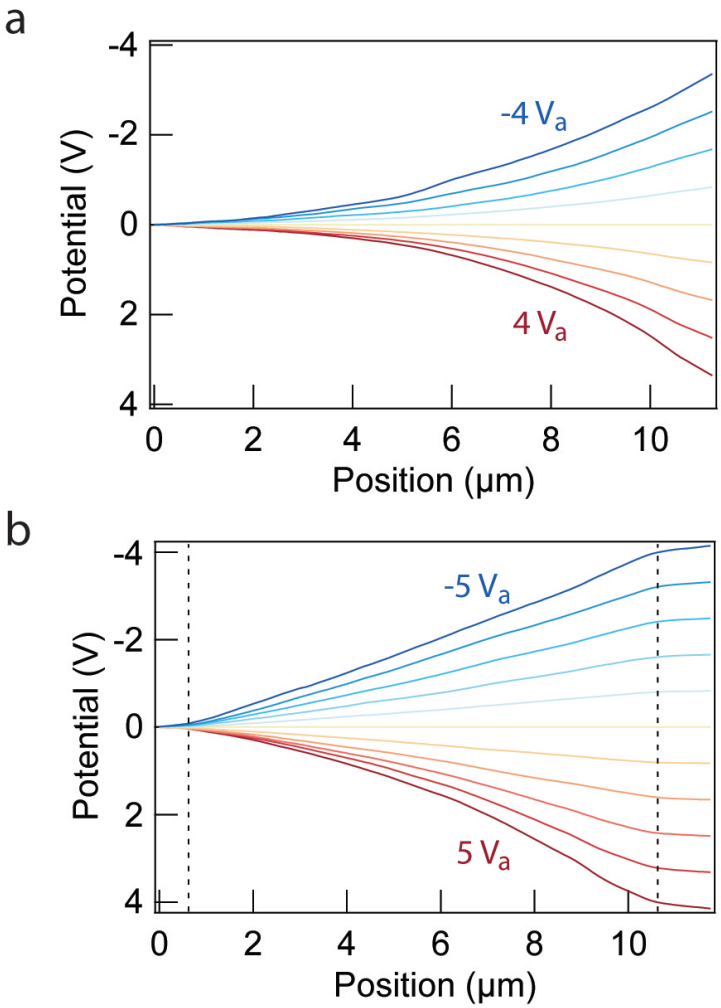

Figure 5.10. Quantitative potential profiles of an n-Si nanowire device before and after surface etching. (a) Electrostatic potential versus position before etching. Profiles were obtained from integrated line profiles of SPCM images which were then scaled to the known potential drop in the channel. Data was taken in 1 V increments from -4 V to 4 V applied bias. Bias was applied to the right contact. (b) Electrostatic potential after etching of the device channel. Dashed lines indicate the edges of the etched region. Data was taken in 1 V increments from -5 V to 5 V applied bias applied to the right contact.

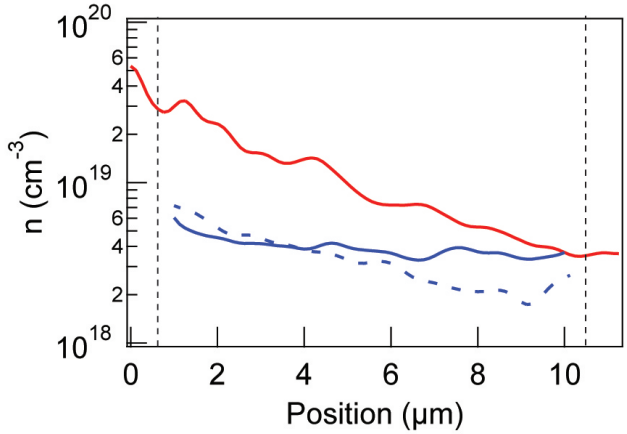

Figure 5.11. Effective electron concentration profiles calculated from the quantitative potential profiles in Figure 5.10a (red) and Figure 5.10b (blue). Solid profiles are averaged over the applied bias range of -4 V to 1 V. The dashed profile is taken from the potential profile of the etched device at 5 V.

The potential profiles can be used to estimate the effective electron concentration profile within the device neglecting any radial variations in the electron concentration. According to Equation 5.11,

$$\mathrm{E(x)} = \frac{\rho(\mathrm{x})}{\mathrm{A(x)}}\mathrm{I_{DC}} = \frac{\mathrm{I_{DC}}}{\mathrm{A}}\frac{1}{\mathrm{n(x)e}\mu_{\mathrm{e}}} \tag{5.14}$$

where n is the effective electron concentration, and μ_e is the electron mobility. Combining with Equation 5.12 and solving for the carrier concentration we have:

$$\mathrm{n(x)} = \frac{\mathrm{I_{DC}}}{\mathrm{I_{ph}(x)}}\frac{\alpha}{\mathrm{e}\mu_{\mathrm{e}}\mathrm{A}} \tag{5.15}$$

The primary uncertainty in this estimate of the effective carrier concentration lies in the mobility, which is not known; a value of 150 $cm^2/V \cdot s$ was used for the plots in Figure 5.11. It would not be prudent to use the field-effect mobility determined by the

transconductance in this instance due to the radially non-uniform doping profile. It is reasonable to assume that the mobility is constant in x because the majority of charge transport likely occurs through the bulk of the wire. The effective carrier concentration profile of the unetched nanowire decays from 4×10^{19} cm^{-3} to 4×10^{18} cm^{-3} moving toward the nanowire tip (Figure 5.11). After etching the carrier concentration is relatively uniform at 4×10^{18} cm^{-3} in agreement with the value of the near-tip region for the unetched wire. At high positive biases, the etched nanowire begins to deplete near the biased contact, as described above. The carrier concentration at 5 V bias is shown in Figure 5.11 as evidence that SPCM will be useful for probing the evolution of carrier concentrations as they are influenced by external potentials as well as intrinsic inhomogeneities.

5.5. Implications for nanowire devices

There are several potential consequences of surface doping, some of which are subtle. As has been pointed out by other authors, the synthesis of complex axial doping profiles is complicated by unintentional radial doping profiles[36,47]. Surface doping may also diminish the influence of surface states on conductivity[49,58] by narrowing depletion layers. Even in the absence of surface states, a radially non-uniform doping profile will create a radially non-uniform potential and could produce carrier confinement at or away from the surface. Finally, considering again the etched device of Figures 5.6, 5.7 and 5.8, one can see that the surface etching will create two n^+-n junctions at the edges of the etch window, and these junctions produce an axial potential gradient that should be detected by SPCM. No peaks are seen in the SPCM profiles of 5.8, indicating that a 2 nm surface etch is insufficient to produce a detectable potential gradient. A 4 nm etch on another device,

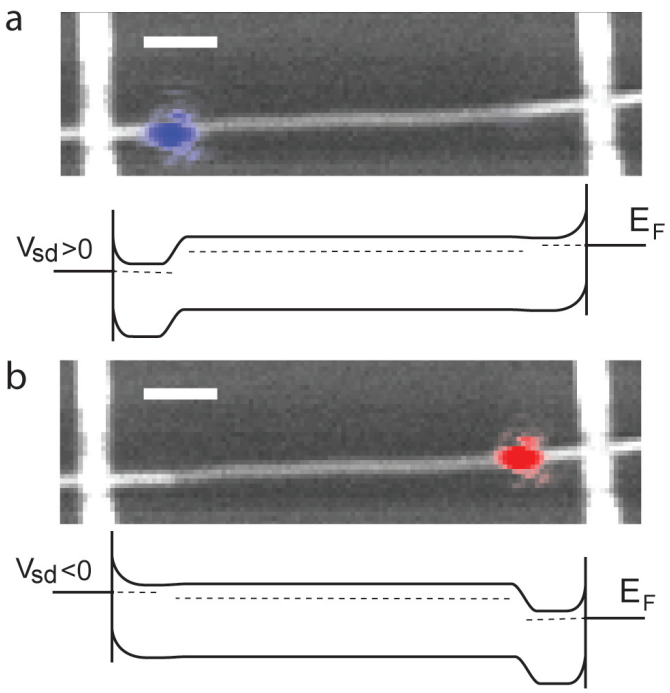

Figure 5.12. SPCM analysis of an n-Si nanowire device with deeply etched (4 nm) channel. (a), (b) Local photocurrent of the device with 2 V and -2 V bias applied to the left contact, respectively. Optical images are displayed as grayscale with the photocurrent signal overlayed in red/blue (±70 nA). Proposed band structures are shown below each image showing the location of the potential drop. The extension of the space-charge regions at the junctions and contacts are exaggerated for display. Scale bars are 2 μm.

however, did result in the formation of potential barriers at the edges of the etch window (Figure 5.12). The photocurrent shows a single strong peak at one edge of the etched region under an applied bias (Figure 5.12a), and a peak of opposite sign is seen at the other edge following bias reversal (Figure 5.12b).

The band diagrams accompanying the SPCM data in Figure 5.12 provide an explanation for the observation of the photocurrent peaks based on the formation of n^+-n junctions. In Figure 5.12a, a positive bias on the left contact puts the left (right) junction

into reverse (forward) bias. As a result, the potential drop occurs primarily at the left junction, and the SPCM signal is localized to this junction because the electric field is very large. Reversing the bias causes the potential drop to occur at the opposite junction. A more detailed analysis of this device and the associated potential profiles are presented in Chapter 6. In the present context, it is noted that nanowire contact regions are often etched to remove a native oxide prior to metal contact evaporation. If surface-doped nanowires are sufficiently etched, barriers such as those shown here may significantly impact the performance characteristics of the devices. This was demonstrated in the previous chapter using EBIC. It is clear from this example that SPCM can play a useful role in elucidating the operating principles of nanowire devices.

5.6. Summary

The results presented in this chapter include advances in both understanding of dopant incorporation in VLS-grown nanowires as well as quantitative applications of SPCM. It was shown that phosphorous-doped silicon nanowires have a nonuniform resistivity arising from a doping profile with enhanced doping at the base of the wire even in the absence of measurable taper. Furthermore, utilizing a four-terminal device geometry it was shown that it is possible to extract quantitative potential profiles of nanowire devices. Before and after potential profiles show that after etching the nonlinear potential profile becomes linear indicating that the resistivity gradient was removed. Finally a simple model of the photocurrent was proposed that enables the calculation of an effective carrier concentration.

Detailed in Chapter 2 is an estimation of surface state density based on surface etching of phosphorous-doped silicon nanowires[58]. Radially uniform doping was a necessary assumption in the calculation which the authors acknowledged required further investigation. The findings presented in this chapter confirm a radial doping profile exists and will significantly impact future studies of nanowire properties and device design.

In this chapter quantitative potential profiles were determined using SPCM. Therefore it is pertinent to compare this approach to Kelvin-probe force microscopy (KPFM) which may also be used to obtain this information. KPFM is a noncontact variant of atomic force microscopy which enables the quantitative measurement of surface potentials. Because KPFM depends only on the electrostatic forces between the tip and the surface, it can be used on a wide variety of materials and can measure non-varying potentials. SPCM, on the other hand, probes the local electric field using generated excess carriers. Therefore its application in determining potentials is limited to semiconductors with a potential gradient. The result is a quantitative measurement of the change in potential in the material rather than a direct measurement of the ground-referenced potential. However, there are also a number of advantages to using SPCM. SPCM involves no physical probe thus reducing the risk of perturbing the sample during measurement. Furthermore, using a long working-distance objective one could potentially conduct SPCM in situations where it may be difficult or impossible to incorporate a direct physical probe.

CHAPTER 6

SPCM analysis of n-Si nanowire FETs fabricated by selective surface etching

The initial push toward the investigation of nanowire-based devices was fueled by the potential for high-performance quasi one-dimensional FETs[3,4]. Nanowire FETs based on silicon are of particular interest because of their compatibility with existing processing technologies. Devices made from uniformly doped p-type and n-type Si nanowires exhibit transistor figures of merit comparable to planar complementary metal-oxide-semiconductor devices[6,53]. These devices face performance trade-offs that limit the ultimate transconductance that can be realized. For lightly doped wires, the series contact resistance limits the transconductance and reduces on-state currents. The contact resistance can be improved by increasing the nanowire doping level, but this significantly increases off-state currents. Recently, high-performance Ge/Si core/shell nanowire heterostructures have been used to fabricate nanowire FETs that outperform state-of-the-art metal-oxide-semiconductor FET (MOSFET) technology in most respects[9], but they also exhibit fairly high off-state currents and ambipolar transport unless asymmetric gate geometries are utilized. An alternative route to high performance nanowire FETs is to replicate typical MOSFET device structures in a single nanowire by in-situ modulation doping of Si nanowires[51] or selective ion implantation[52]. Both approaches show significant improvements over uniformly doped nanowire FETs, but require high-temperature

annealing and prior removal of the Au catalyst. The modulation doped device also creates a challenge for alignment to the channel region.

In this chapter, the fabrication and characterization of a new type of Si nanowire FET will be presented. The device is based on surface etching of the device channel in surface-doped nanowires to reduce contact resistance and enhance transconductance. Back-gated devices show good transistor performance with on/off ratios of 10^6 and field-effect mobilities as high as 525 $cm^2/V \cdot s$. I-V characteristics were correlated with SPCM measurements to follow the evolution of potential profiles under various operating conditions. Based on this analysis, the extent to which the nanowire transistor conforms to or deviates from that of a conventional MOSFET will be discussed.

6.1. Device performance of n-Si nanowire FETs

The Si nanowires used in this study were fabricated by low-pressure chemical vapor deposition with mono disperse 50 nm Au particles as catalysts for vapor-liquid-solid (VLS) growth. The source gases, SiH_4 and PH_3, were combined in the reactor at a ratio of 500:1 to produce n-type Si nanowires with enhanced surface doping. Verification of the surface doping is presented in Chapter 5. Detailed growth conditions can be found in Appendix C. The fabrication and characterization of devices using the as-grown nanowires will be detailed before discussing the etched FETs. The final etched FET devices were fabricated by etching the channel region of a surface-doped nanowire resulting in an n^+-n-n^+ structure like those presented in Chapter 5. Four-terminal devices on single nanowires were fabricated using EBL and contact metalization with Ni/Ti. Prior to metal evaporation, the contact area was treated with oxygen plasma to remove residual

resist and a 7-second wet etch with buffered-HF solution to remove the native oxide. Four-probe device measurements on intact nanowires showed low contact resistances of 3 to 6% of the total two-terminal resistance. The central channels in the four-probe devices were made with lengths of $> 10\ \mu m$ to simplify SPCM analysis as discussed below. As-fabricated devices showed little current modulation with the application of a gate bias and the field-effect mobility (calculated using the method presented in Chapter 3) ranged from 26 to 34 $cm^2/V \cdot s$. Carrier concentrations can be estimated from the measured resistivity and field-effect mobility using the relation $n = 1/\rho e\mu$ and ranged from 5-6$\times 10^{19}$ cm^{-3} consistent with previous estimates in wires with similar growth conditions[38]. However, it must be stressed that the field-effect mobility is a device parameter and is not necessarily equal to the carrier mobility in the nanowire. Therefore the reported carrier concentration is merely a rough estimate.

Surface etching in the channel region dramatically improved the gate response. Selective etching was realized by coating samples with a 1 μm-thick layer of PMMA and defining windows by EBL in the middle channel of the four-probe devices. The PMMA protects the contacts and ensures that the nanowire is etched only in the exposed region defined by the window. Wet chemical etching with NH_4F for 20s removed 2 to 4 nm of the nanowire surface across multiple devices after removing the native oxide with buffered HF. The resistance of etched devices increased disproportionately to the decrease in diameter, consistent with the removal of dopants near the surface. Devices with 4 nm of surface etching showed improved FET behavior. Field-effect mobilities increased by factors of up to 20, and on/off ratios of 10^6 were observed. Using adjusted values for the channel length and wire diameter, and assuming that the etched region dominates transport, the

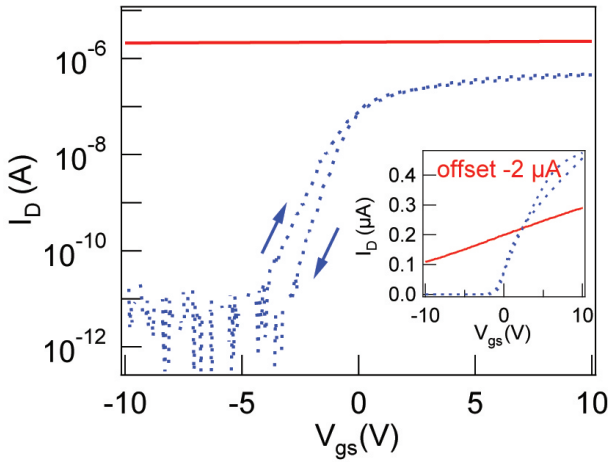

Figure 6.1. Device transfer curves of an n-Si nanowire FET before (red, solid) and after (blue, dashed) etching. The main plot is on a semi-log scale to show the subthreshold characteristics while the inset is on a linear scale to demonstrate the improvement in conductance. The before etching data is offset by -2 μA on the linear scale for comparison. Arrows on the main plot indicate sweep direction.

estimated carrier concentration after etching was ~2×10^{18} cm^{-3} based on the average field-effect mobility (175 $cm^2/V \cdot s$ for this device) and the resistivity calculated from the two terminal resistance at 0 V_g. Figure 6.1 shows the transfer characteristics of an n-Si nanowire device before and after surface etching. Hysteresis in the gate response was < 1 V and the maximum subthreshold slope was 600 mV/dec. We note that the device measurements shown here were taken 3-4 days after etching to allow a native oxide to re-form, as characteristics immediately following etching were quite distinct. Qualitatively, freshly etched devices showed large hysteresis in the gate response and reduced on-state currents, whereas after 3-4 days the on-state current increased by a factor of 2-3, the hysteresis reduced dramatically, and the subthreshold slope improved. Additional studies will be necessary to document and understand the evolution of this behavior.

The operating principles of these etched n-Si nanowire FETs are similar to a conventional floating-body MOSFET although the dopant type of the device channel is the same as that of the source and drain region. As a result, an n^+-n junction limits the current in the off state rather than a p-n junction. The reduced barrier height has consequences for the currents in both saturation and depletion. N-channel MOSFETs show strong saturation in I_D versus V_{DS} for $V_{DS} > (V_{gs} - V_{th})$ due to channel pinch-off arising from electrostatic interaction with the gate electrode. However, the etched n-Si nanowire FETs show significant leakage in the saturation region of the I_D versus V_{DS} data (Figure 6.2a) probably due to the small barriers between channel and drain.

In typical planar MOSFET devices, there are a number of models that can be used to describe the current-voltage behavior. For the type of nanowire FET used in this study, the quadratic model may be used as it accounts for the variation in charge accumulation along the length of the device due to the difference in potential at the source and drain, but does not include any additional factors that are specific to the traditional MOSFET geometry. The expression for the MOSFET drain current given by the quadratic model is

$$I_{DS} = \frac{d\mu C_{ox}}{2L}\left[2(V_g - V_{th})V_{DS} - V_{DS}^2\right];\ for\ V_{DS} < V_g - V_{th} \tag{6.1}$$

$$I_{DS,sat} = \frac{d\mu C_{ox}}{2L}(V_g - V_{th})^2;\ for\ V_{DS} > V_g - V_{th}, \tag{6.2}$$

where μ is the majority carrier mobility, C_{ox} is the oxide capacitance, L is the channel length, and V_{th} is the threshold voltage. For $V_{DS} > V_g$-V_{th}, the channel is depleted near the drain causing current saturation where the drain current is given by $I_{DS,sat}$. The red dashed lines in Figure 6.2 are fits to the data using this model. The oxide

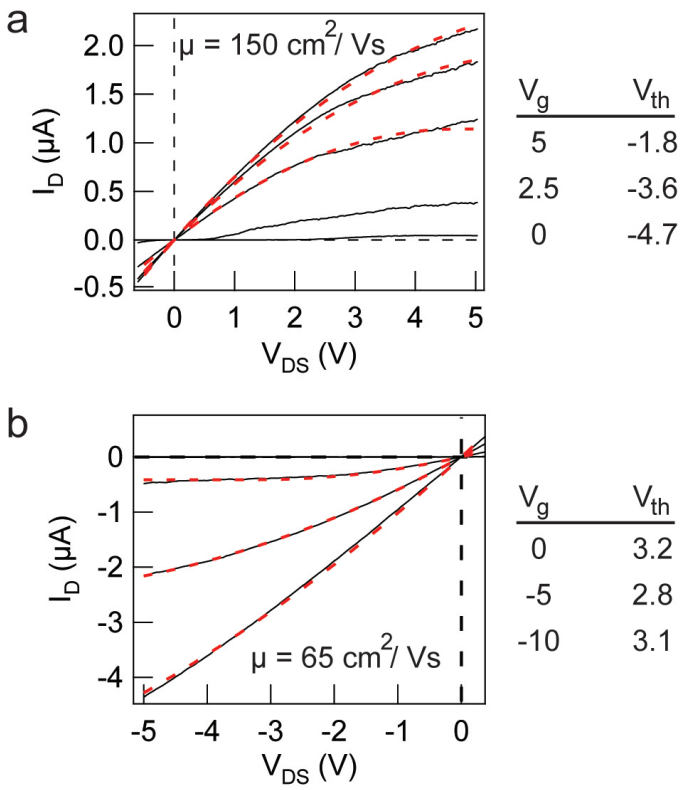

Figure 6.2. I-V data for etched n-Si, (a), and unetched p-Si, (b), nanowire FETs at different gate biases. Red dashed lines are fits to the data using the quadratic model for MOSFET drain current. The table to the right of each plot gives the applied gate bias and the threshold voltage determined from the fits.

capacitance was approximated using the corrected cylinder-on-plane model presented in Chapter 3 and the mobility was assumed to be equal to the bulk value (~ 150 cm^2/Vs for n=3×10^{18} cm^{-3}). The inset of Figure 6.1 indicates a V_{th} of approximately -2 V. However, the quadratic model indicates a shifting V_{th} from -1.8 V at V_g = 5 V to -4.7 V at V_g = 0 V. This does not necessarily represent a shift in the actual threshold, but rather indicates that the drain current is significantly higher than expected at high V_{DS}. For comparison, current-voltage data for a p-type silicon nanowire FET is shown in Figure

6.2b. In this case the data matches very closely with the quadratic model and the current saturates as expected for $V_{DS} > V_g\text{-}V_{th}$. In this device, current modulation in the on-state is controlled by the carrier concentration in the nanowire while the subthreshold characteristics are determined by barriers at the metal-semiconductor junctions which typically have barrier heights of 0.3 to 0.8 eV. Therefore, deviation from the model in etched n-Si nanowire FETs is likely due to incomplete current saturation from the small n^+-n junctions. The explanations of device behavior thus far have been based only on I-V characteristics and assumptions made regarding the effects of surface etching. In the next section, SPCM is used to confirm the mechanisms controlling the device as well as investigate potential profiles at high V_{DS}.

6.2. SPCM investigation of device operation

SPCM measurements were performed using a confocal microscope to focus above-bandgap (532 nm) illumination onto a sample mounted on a piezoelectric scanning stage. Additional information about the details of the measurement are given in Chapter 3. Drift of the excited carriers in the presence of an electric field results in a measurable change in device current. SPCM is sensitive to local electric fields within the device and can be used to observe changes in the relative magnitude of fields during device operation.

Correlation of the device transfer curve with SPCM results confirms that the back gate effectively modulates the conductivity of the etched portion of the nanowire in accumulation, and that the n^+-n junctions control device performance in the subthreshold regime. The photocurrent map for an etched n-Si nanowire FET in strong accumulation at $V_{DS} = 0.5$ is shown in Figure 6.3b; light regions indicate a positive photocurrent. Photocurrent is

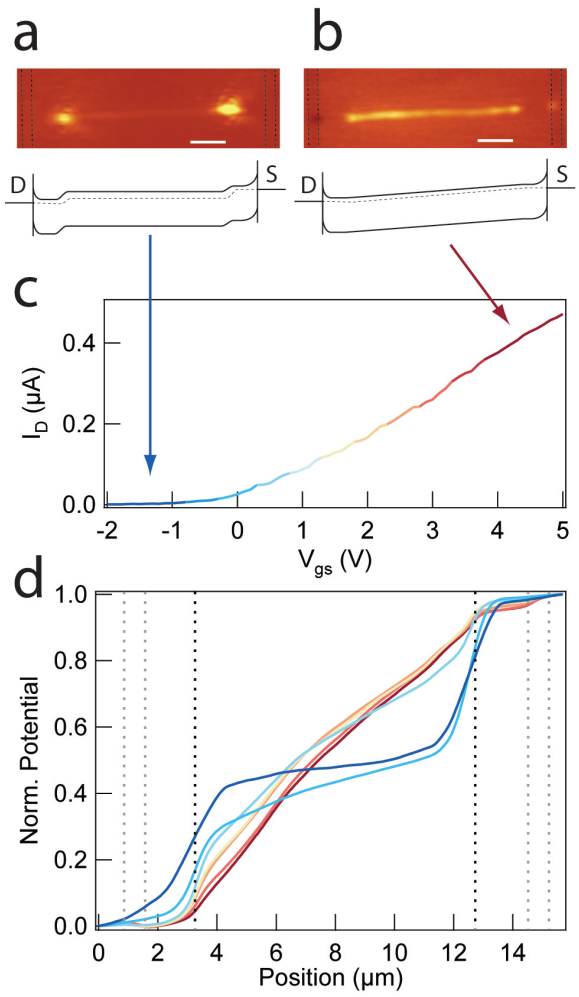

Figure 6.3. Correlation of SPCM analysis and device transfer characteristics. (b),(c) Photocurrent images and proposed band structures for the device with $V_{DS} = 0.5$ with the drain electrode on the left. Arrows indicate the location on the transfer curve that the images were taken. Dashed lines on the image indicate the location of the contacts and all scale bars are 2 μm. (d) Transfer curve for the nanowire FET with $V_{DS} = 0.5$. The plot is colored to correspond to the potential profiles in 'e'. (e) Normalized pseudo potential profiles taken at different V_{gs} with $V_{DS} = 0.5$. V_{gs} is indicated by the trace color corresponding to the colors in 'd'. Light dashed lines indicate the location of the contacts and dark dashed lines mark the edges of the etched region.

observed across the entire etched portion of the device with no signal in the unetched region. Given that $I_{PC} \propto E(x) = -dV(x)/dx$, the SPCM image confirms that the potential drop is occurring within the channel, producing a uniform electric field. When the gate voltage is lowered below the device threshold voltage value, the photocurrent response in the channel becomes negligible compared to the edges of the etched regions where large peaks appear (Figure 6.3a). The peaks are indicative of the significant potential gradient associated with the n^+-n junctions when the channel region is depleted as indicated in the schematic band structure in Figure 6.3a. Furthermore, qualitative potential profiles can be obtained by integrating the photocurrent along the device channel. Normalized qualitative profiles are then used to follow the band structure across many biasing conditions[66]. Normalized potential profiles of the device at $V_{DS} = 0.5$ reveal the evolution of the device as it is brought from depletion to accumulation (Figure 6.3e). In depletion and at moderate source-drain bias, the potential within the device channel is flat with nearly symmetric potential drops observed at the n^+-n junctions. As the gate bias is increased and the channel brought into accumulation, the barriers at the n^+-n junctions are reduced, and a potential drop appears in the device channel. In strong accumulation the potential profile in the channel is nearly linear with negligible contribution from the junctions. Because of the high doping in the unetched regions of the wire, the external field applied by the back gate has little effect on the Fermi level in those regions. The conductance modulation is therefore accounted for by the modulation of the Fermi level within the etched region. At gate voltages below threshold, the large difference in Fermi energy between etched and unetched regions gives rise to a space charge region and a corresponding potential barrier for majority carriers. SPCM analysis therefore confirms

conventional MOSFET operation in depletion and accumulation at moderate source-drain biases. Next, saturation at increased drain bias will be considered.

Saturation occurs in MOSFETs when $V_{DS} > (V_{gs} - V_{th})$) and the depletion of carriers close to the drain creates pinch-off in the adjacent channel. SPCM analysis confirms that saturation in the drain current in etched n-Si nanowire FETs also arises due to depletion of the device channel near the drain (n^+-n junction). I_D versus V_{DS} for V_{gs} = 5 corresponding to accumulation is plotted in Figure 6.4b. The drain current shows saturation at V_{DS}= ~5 and is linear at negative bias. The photocurrent map at negative bias shows a uniform response within the etched portion of the device (bottom image of Figure 6.4a). In this condition, the channel conductance is enhanced by the applied gate bias so that the potential drop occurs uniformly. As the drain current begins to deviate substantially from a linear trend (Figure 6.4b), increasing photocurrent is observed near the drain junction (Figure 6.4a, middle image) indicative of an increasing electric field. At V_{DS} = 4, the drain current appears to saturate weakly, and the photocurrent map shows only a single peak at the drain-side n^+-n junction (top image of Figure 6.4a). Upon comparison of the potential profiles taken at different V_{DS} (Figure 6.4c) to the I_D-V_{DS} plot (Figure 6.4b), it is clear that potential drop is increasing adjacent the drain as the drain current begins to saturate with increasing V_{DS}. The shape of the potential profiles in saturation closely match those measured in typical MOSFETs[86], suggesting that the etched n-Si nanowire FETs operate like a typical MOSFET up to the point of saturation. As mentioned previously, however, the drain current continues to increase beyond the nominal saturation voltage. SPCM profiles can also provide some insight into the weak saturation behavior.

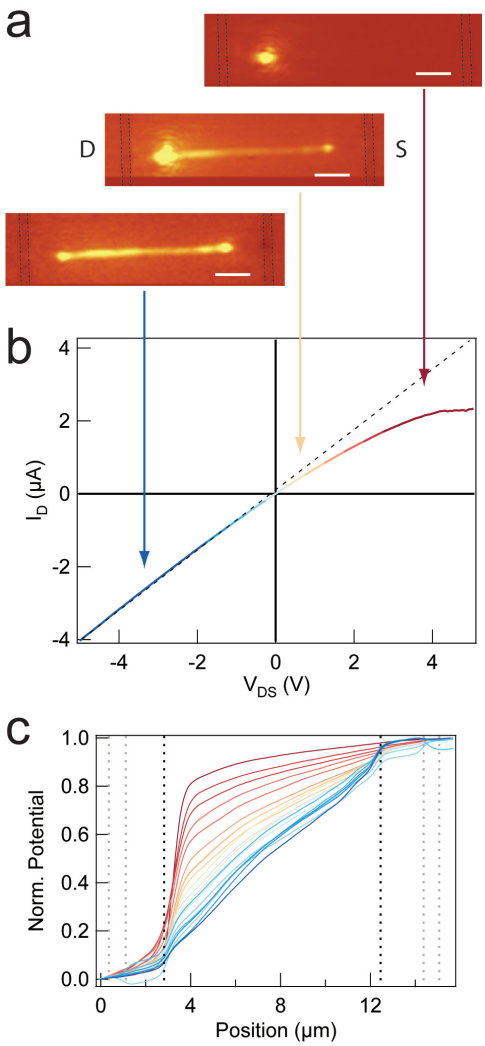

Figure 6.4. Correlation of SPCM analysis and I_D versus V_{DS} at $V_{gs} = 5$. (a) Photocurrent images taken at different V_{DS} indicated by the arrows to the I_D versus V_{DS} plot in 'b'. The drain electrode is on the left. Dashed lines indicate the location of the contacts and all scale bars are 2 μm. (b) I_D versus V_{DS} curve taken at $V_{gs} = 5$. The plot is colored to correspond to the potential profiles in 'c'. The dashed line is a guide for the eye showing a continuation of the linear trend observed at negative V_{DS}. (c) Normalized pseudo potential profiles taken at different V_{DS} with values indicated by the trace color corresponding to the colors in 'b'. Light dashed lines indicate the location of the contacts and dark dashed lines mark the edges of the etched region.

Local photocurrent maps taken at high bias ($V_{DS} > (V_{gs} - V_{th})$) reveal an electric field within the etched region of the device near the drain side indicating that the potential drop in the device does not occur only at the n^+-n junction. The I_D versus V_{DS} plot at $V_{gs} = 0$ is shown in Figure 6.5b. Again the drain current is linear at negative applied drain-source bias, but now the saturation occurs at $V_{DS} = \tilde{}3$. The observed increase in drain current as V_{DS} increases beyond the point of saturation is not desirable and indicates leakage through the n^+-n junction. The SPCM images in Figure 6.5a show clear differences from the previous case when the channel was in strong accumulation. At negative V_{DS} there is now only a single photocurrent peak at the source-side n^+-n junction (bottom image in Figure 6.5a). At $V_{gs} = 0$ the device is very close to the threshold voltage, so it is not surprising that we now see a strong field at one of the junctions. The peak appears at the source-side of the device because a negative bias is applied at the drain effectively forward-biasing the drain-side junction and reverse-biasing the source-side junction. Once the drain bias is positive, this condition is reversed and the peak shifts to the drain-side junction (middle image in Figure 6.5a). At high V_{DS} the photocurrent map shows signal within the etched region near the drain side of the device (top image of Figure 6.5a). The color scale has been changed for this image in order to give better contrast. The apparent increase in signal at the source-side junction is an artifact of this change. The normalized pseudo potential profiles in Figure 6.5c show that there is no change in the relative contribution from the source-side junction. The signal extending into the etched region from the drain increases both in magnitude and extent with increasing drain current. The shape of the potential profile in the channel represents the resistivity profile arising from carrier depletion toward the drain side. The

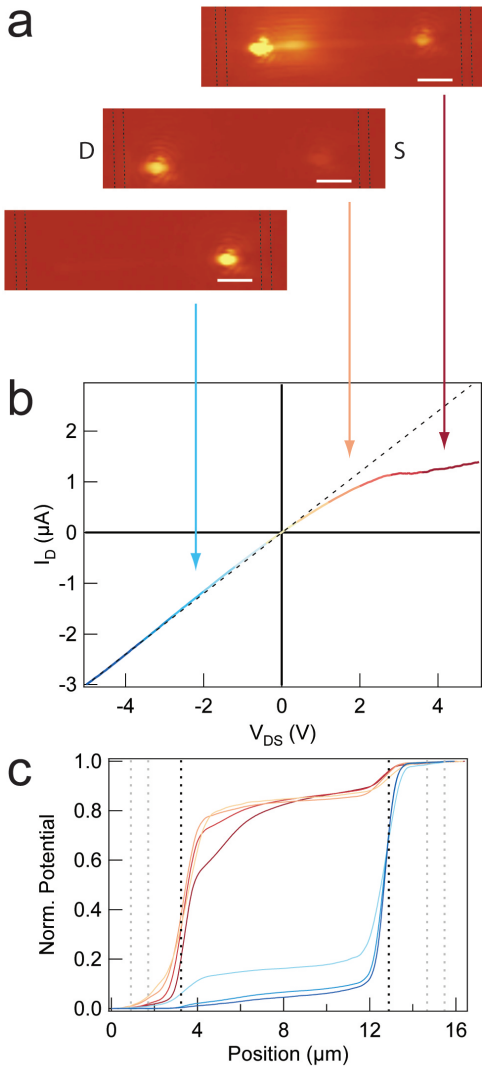

Figure 6.5. Correlation of SPCM analysis and I_D versus V_{DS} at $V_{gs} = 0$. (a) Photocurrent images taken at different V_{DS} indicated by the arrows to the I_D versus V_{DS} plot in 'b'. The drain electrode is on the left. Dashed lines indicate the location of the contacts and all scale bars are 2 μm. (b) I_D versus V_{DS} curve taken at $V_{gs} = 0$. The plot is colored to correspond to the potential profiles in 'c'. The dashed line is a guide for the eye showing a continuation of the linear trend observed at negative V_{DS}. (c) Normalized pseudo potential profiles taken at different V_{DS} with values indicated by the trace color corresponding to the colors in 'b'. Light dashed lines indicate the location of the contacts and dark dashed lines mark the edges of the etched region.

potential drop at V_{DS} = 3 V extends ~3 μm into the channel while for V_{DS} = 5 V it extends ~4 μm consistent with increased carrier depletion in the channel with increasing V_{DS}. Conventional n-type MOSFETs use an n^+-p-n^+ structure that is normally off. The gate electrode is used to create an inversion layer in the p-type material thus providing a conduction path for electrons. In this type of structure, barriers at the p-n junctions effectively block electron transport when the device is in the off-state. As with the metal-semiconductor junction in the p-Si nanowire FET, the barriers at p-n junctions of an n-MOSFET can be significantly larger than the n^+-n junctions in the etched nanowire devices presented here.

6.3. Summary

The results presented in this chapter include a new approach toward the fabrication of high-performance nanowire FETs using uniformly doped silicon nanowires. Devices show significant improvements over previously reported uniformly doped nanowire FETs with on/off ratios of 10^6 and field-effect mobilities as high as 525 $cm^2/V \cdot s$. Investigation of device operation using SPCM confirms that the performance of surface-etched n-Si nanowire FETs depends on the modulation of n^+-n junctions introduced at the edges of the etched region. This is analogous to the operation of conventional MOSFET devices. Previous reports on silicon nanowire FETs have indicated reduced device performance because of the series resistance introduced at the contacts. In this work this problem was avoided by contacting heavily doped segments of the nanowire to reduce contact resistance.

Device performance may be improved further using relatively simple changes to the device fabrication process. One suggestion would be to use a top-gated structure. A top-gate would provide significant improvement in gate coupling with a conformal interface over a much larger fraction of the nanowire surface area. Furthermore, a n^+-p-n^+ structure could be fabricated by first growing a lightly doped p-Si nanowire and depositing a heavily doped n-type shell. After device fabrication and surface etching, the result would be an inversion-mode nanowire FET closely resembling a conventional MOSFET structure.

An outstanding question in this work is the effect of the NH_4F etching on the surface properties. As was mentioned above, devices immediately after etching show large hysteresis and reduced on-state currents. After 3-4 days in air performance improves significantly. From conventional knowledge, one would expect improved performance immediately after etching as the surface should be H-passivated. Reduction in surface states should lead to reduced hysteresis and higher current. As the H-passivation destabilizes a native oxide will form returning the surface to its previous state. Ensemble XPS studies of the nanowire surface after etching could be used to confirm the time scale of oxide regrowth and may be correlated with device performance.

CHAPTER 7

SPCM analysis of p-Si nanowire FETs with intruded $NiSi_x$ contacts

Recent reports of Raman spectroscopy studies of boron-doped silicon nanowires have shown evidence of enhanced carrier concentration at the nanowire base[57]. Furthermore, diborane, a common source gas for boron dopants, has been shown to have significant effects on VLS growth of silicon nanowires through enhancement of silane decomposition at the nanowire surface[35,39]. In this chapter, p-type nanowire FETs fabricated using boron-doped silicon nanowires will be characterized by correlating current-voltage characteristics with SPCM analysis. Multiple devices were fabricated along a single nanowire to investigate the influence of surface doping on device performance. It was found that the threshold voltage decreases monotonically from the base to the tip of the nanowire consistent with increased carrier concentration at the base. Correlation with SPCM results show that for devices near the nanowire tip, contact resistance plays a larger role in the transport than for devices near the base. While threshold voltage and subthreshold slope scale as expected for surface doping, the calculated field-effect mobility does not show any clear trend, possibly due to variations in the contact resistance along the wire. Finally, SPCM analysis of a long-channel p-type silicon nanowire FET reveals that only ~1.5 μm of the 5 μm channel is effectively modulated by the back-gate electrode. In

the typical field-effect mobility analysis, this results in a significant overestimation of the carrier mobility and has broad implications for nanowire device performance analysis.

Low-resistance contacts to lightly boron-doped p-type silicon nanowires were fabricated by EBL and subsequent nickel evaporation. Rapid thermal annealing resulted in intruded $NiSi_x$ segments which provide lower contact resistance and improved interface quality, as described in Chapter 3. Typical intrusion length was approximately 500 nm. The wires used in this study have a measurable taper of ~0.4 nm/μm arising from radial VS deposition of silicon. It is expected from previous results[57] that, in addition to the change in diameter, there will be a carrier concentration profile arising from dopant incorporation during VS deposition.

7.1. Spatial variation of device performance

In order to investigate the effect of surface doping on device performance, four devices were fabricated along a 12 μm-long boron-doped silicon nanowire. The spacing of the EBL-defined electrodes was ~1.8 μm as shown in Figure 7.1. After annealing, an intruded $NiSi_x$ segment is formed with an intrusion length of 500 nm. The result was a series of p-type nanowire FETs with 800 nm channel lengths and axial metal-semiconductor junctions at the contacts.

7.1.1. Current-voltage analysis

Figure 7.1b shows the transfer characteristics of four p-FETs along a single nanowire. Devices are numbered 1 to 4 going from the tip of the wire to the base. All four showed p-type transport behavior with all but device 4 able to be depleted to an off-state current

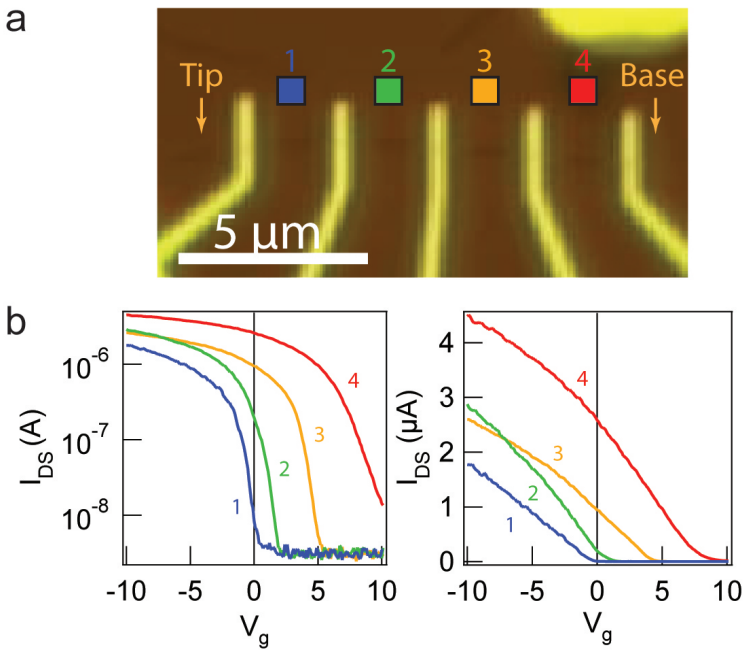

Figure 7.1. I-V_g characterization of a 5-terminal p-type silicon nanowire device. (a) Optical image of the device. The four two-terminal devices are numbered in order from the tip of the wire to the base. Colored squares provide color-coded association with the data in 'b'. (b) Transfer characteristics of the devices pictured in 'a'. Plot color corresponds to the colored squares in 'a'. Data is presented on a semilogarithmic (left) and linear (right) scale to show both the subthreshold characteristics as well as the conductance.

equal to the noise level of the measurement setup withing the range of applied V_g. For a p-type FET, the threshold voltage is the voltage required to turn off the device. In this case, the threshold voltage was found to decrease toward the tip of the nanowire with the lowest value being below zero (see Figure 7.2a). Therefore the device at the tip of the nanowire was an enhancement-mode FET and is off in the absence of an applied gate bias while the other three were depletion-mode FETs. This confirms a decreasing carrier concentration towards the tip of the nanowire. Also plotted in Figure 7.2a is the subthreshold slope. At the base of the nanowire the subthreshold slope was 2.1 V/dec

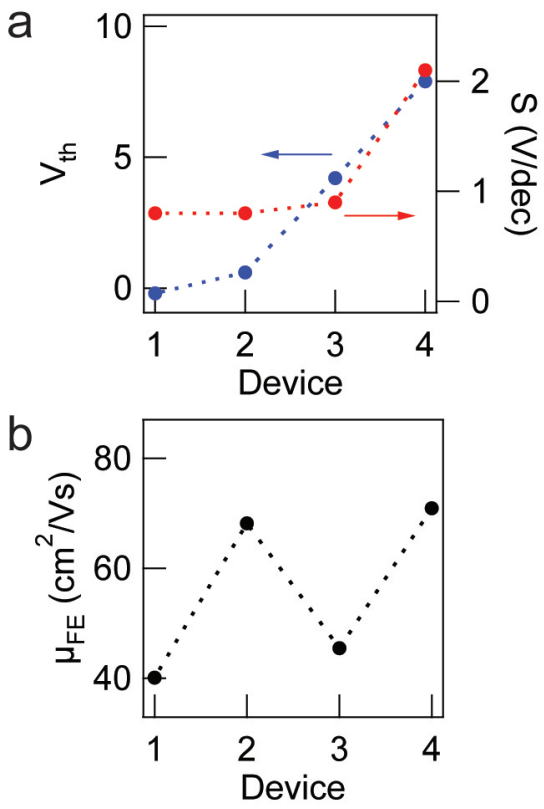

Figure 7.2. Device parameters for p-type silicon nanowire FETs along the nanowire length. (a) Threshold voltage, V_{th}, (left axis) and subthreshold slope, S, (right axis) for devices 1 to 4. (b) Field-effect mobility for devices 1 to 4. The nanowire tip is closest to device 1 with 4 being near the base of the nanowire.

compared to 0.8 V/dec near the tip. This degradation in performance at the base can be attributed to reduced carrier modulation in the channel because of a high density of charges at the surface that act to screen the external electric field. With decreased carrier concentration toward the tip of the nanowire, there should be a corresponding increase in carrier mobility. As discussed in Chapter 2, there are not methods to directly measure the mobility. Instead the field-effect mobility was calculated for each of the

devices. The general procedure for this calculation is presented in Chapter 3. Figure 7.2b shows the field-effect mobility for each of the devices. In this case the field-effect mobility did not scale as expected with doping level but rather showed no clear trend with position. The reason for this is not clear, however previously reported results on uniformly doped n-type silicon nanowire FETs showed that the field-effect mobility is sensitive to the contact resistance with increased contact resistance leading to a decreased field-effect mobility[53]. It is possible that variations in the contact resistance along the length of the wire influenced the observed mobility scaling. Because of the annealing process used for these devices, four-probe measurements are not possible, so contact resistance cannot be directly determined. However, SPCM can be used to probe the local electric field in the devices to investigate contact effects.

7.1.2. SPCM of five-terminal device structure

For all four of the devices, SPCM measurements taken at 0 V applied bias showed photocurrent peaks at both contacts (see Figure 7.3a). Peaks were of opposite sign at either end of the devices consistent with internal fields introduced by the metal-semiconductor Schottky contacts[66]. For devices 3 and 4, the peaks were of equal intensity. Devices 1 and 2, closer to the tip of the wire, showed asymmetric peaks with the tip-end peak being higher intensity. Increased photocurrent at the tip-end Schottky contact was likely a result of increased contact resistance resulting from an increase in the depletion width. Upon illumination, excess carriers result in a measurable photocurrent when an internal electric field causes carrier drift. At metal-semiconductor junctions, the extent of the space-charge region depends on the semiconductor doping level. Therefore, for lower doping, the extent

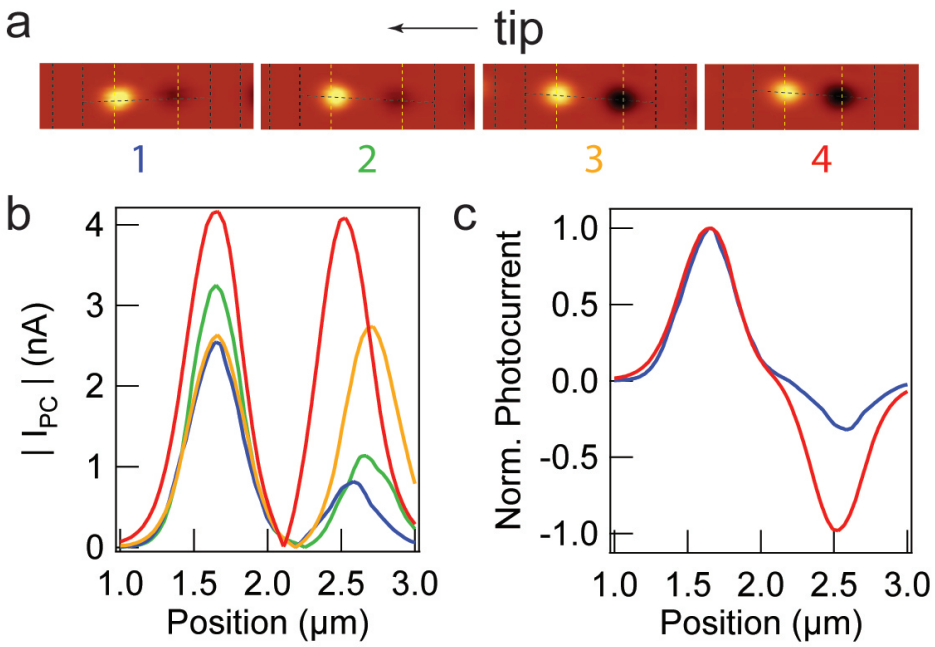

Figure 7.3. Local photocurrent maps of p-type silicon nanowire FETs along the nanowire length taken at 0 V bias. (a) SPCM images of all four devices. The absolute current scales are different for each image, but it can be seen that for devices 1 and 2 the signal at the tip-end contact is greater while for devices 3 and 4 the peaks are symmetric. (b) Photocurrent line profiles of devices 1 through 4 taken at 0 V applied bias. (c) Normalized line profiles of the SPCM images for devices 1 and 4 from 'a' showing asymmetric peak intensity for device 1.

of the internal electric field will be larger which can lead to enhanced collection of excess carriers at the junction. Also of importance is the resistance of the contact opposite the excitation. As excess minority electrons are created in the near-contact region they are collected at the internal electric field; however, by the continuity requirement, there must be equal transport of holes to the opposite contact. Toward the base of the nanowire, the photocurrent signal was equal at both contacts suggesting that the contacts were symmetric. As with the devices at the tip of the device, a surface doping gradient exists.

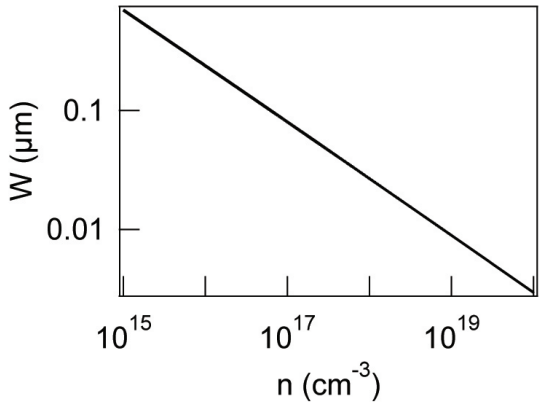

Figure 7.4. Depletion width versus electron concentration for an unbiased p-Si - NiSi Schottky barrier.

However, in this case the doping level was sufficiently high that the difference in depletion width was small and did not significantly affect the contact resistance. Figure 7.4 shows calculated values for the depletion width, W, of the p-Si - $NiSi_x$ junction versus electron concentration. Since the phase of the silicide is not known, the work function for NiSi (4.7 eV) was used. This plot shows that in the expected doping range for the wires studied (1×10^{17} cm^{-3} to 1×10^{20} cm^{-3}) the change in depletion width is small even for a large change in doping concentration.

In addition to the unbiased photocurrent, SPCM can be used to probe the local electric field in the devices under an applied bias. At low applied biases, it was found that for the devices at the nanowire tip the potential drop occurs at the reverse-biased Schottky contact. Devices at the base show an electric field within the device channel even at low applied bias. Figure 7.5 shows the pseudo potential profiles for devices 1 and 4 obtained by integrating line profiles of the SPCM image. Further details concerning the analysis of SPCM data is given in Chapter 5. The dashed lines in the plots mark the location of

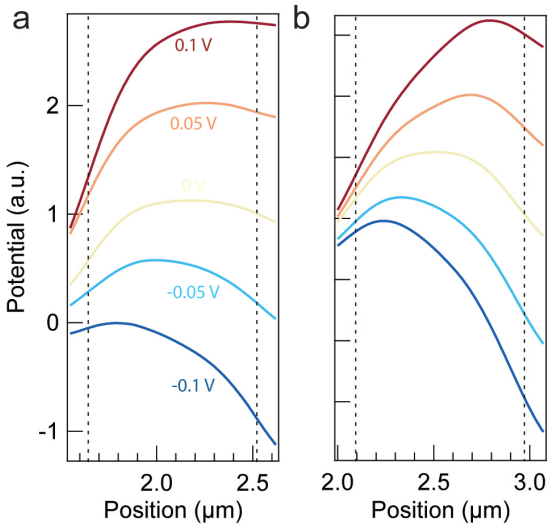

Figure 7.5. Pseudo potential profiles taken from SPCM data of p-type nanowire FETs at the tip, (a), and base, (b), of a boron-doped silicon nanowire. Dashed lines indicate the position of the intruded metal-semiconductor junctions. Voltage values in 'a' are the applied source-drain bias.

the metal-semiconductor junctions. For device 1 (near the tip), a steep potential drop was observed near the left contact at positive bias and the right contact at negative bias. The slope of the potential in the middle of the channel is near zero and does not vary much with applied bias. This indicates that the potential drop occurs primarily at the reverse-biased contact at low applied bias, and that the reverse-biased contact is the dominant resistance. In comparison, the slope of the potential profile of device 4 showed a much larger variation for low applied bias indicating a reduced influence of the contact resistance. It should be noted that the channel length (800 nm) was very short in these devices and approached the resolution of the technique (~500 nm). As a result, it is not possible to completely separate the signal arising from a potential drop at the contact

and signal from the channel of the device. Long-channel devices can be used to study the signal in the channel of a p-type silicon nanowire FET.

7.2. SPCM analysis of a long-channel p-Si nanowire FET

A single long-channel p-type nanowire FET was made using the same fabrication methods described above. After silicide formation, the device channel length was ~6 μm. Current-voltage characterization of the device gives parameters similar to those for the short channel devices with $S = 1.7\ V/dec$, $V_{th} = 5\ V$, and $\mu_{FE} = 96\ cm^2/V \cdot s$. Wire diameter measurements showed a 2 nm taper within the device channel with a 31 nm diameter closer to the base and 29 nm near the tip. An average value of 30 nm was used for calculation of the field-effect mobility. SPCM measurements were used to observe the local electric fields within the device channel.

As with the short-channel devices, the long-channel device showed peaks at both contacts with a larger peak near the nanowire tip (see Figure 7.6) Under an applied source-drain bias, a photocurrent response was observed within the device channel. As with the long channel n-type devices presented in Chapter 5, the maximum photocurrent response was observed closer to the nanowire tip because of an enhanced electric field arising from an increase in resistance in this region. For these wires the increased resistance was attributed to a geometrical factor in addition to surface doping.

Correlation of the transfer characteristics of the device with SPCM results revealed an additional consideration in the analysis of device performance. It was found that when depleting the nanowire channel, the local photocurrent response near the base of the wire almost disappears completely while the signal at the tip is dramatically enhanced

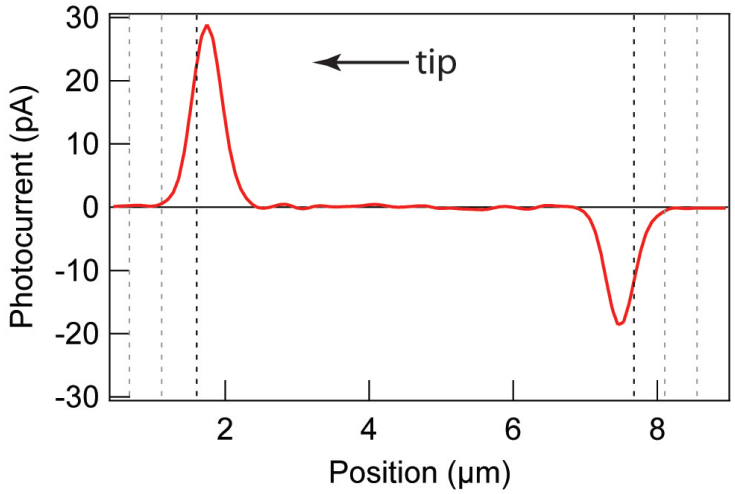

Figure 7.6. SPCM line profile of an unbiased long-channel silicon nanowire p-FET. Grey dashed lines mark the position of the lithographically defined contacts while black dashed lines mark the metal-semiconductor junction of the intruded contacts.

(see Figure 7.7). The normalized pseudo potential profiles in Figure 7.7b show that the potential drop in the channel is localized to the near-tip region for positive gate bias. This is consistent with the results in the previous section on short-channel devices where it was found that devices near the tip were more easily turned off with the back-gate electrode. In this case there could be significant implications for the analysis of device performance. For the calculation of the field-effect mobility it was assumed that the carrier concentration within the device channel was being modulated uniformly. The value of $\mu_{FE} = 96\ cm^2/V \cdot s$ was calculated using 6 μm for the channel length. The SPCM results, however, indicated that the 1.5 μm segment of the device near the tip dominates the device resistance (see inset of Figure 7.7. Therefore, the field-effect mobility should be altered to reflect the effective device channel length. To illustrate this point, the remaining 4.5 μm of the device channel will be treated as a constant series resistance to see what effect that

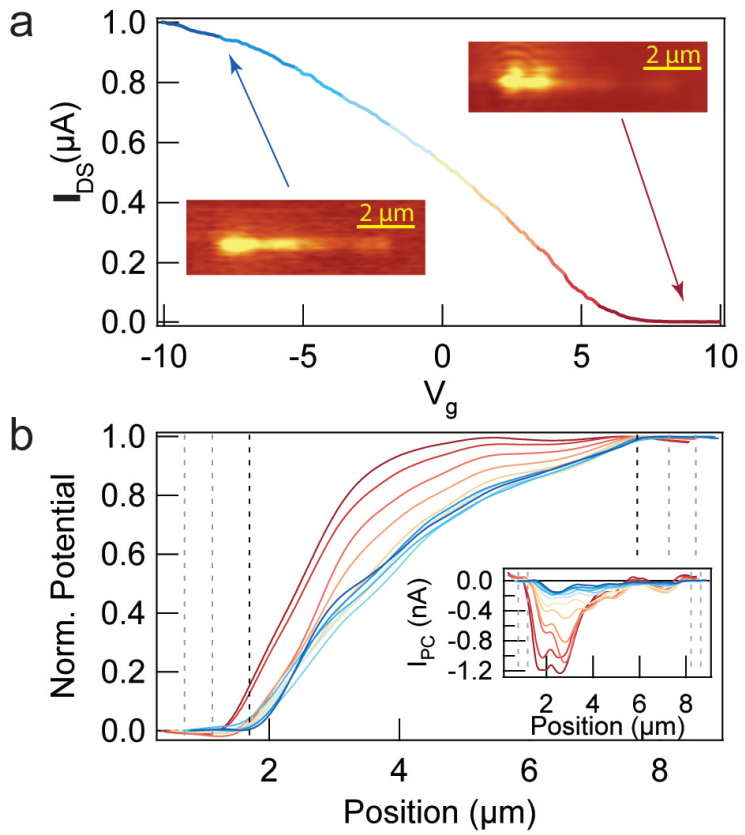

Figure 7.7. Correlation of device transfer characteristics and SPCM line profiles for a long-channel p-type silicon nanowire FET. (a) Device transfer curve and SPCM images taken in accumulation and depletion. Current scale for the image in accumulation is ±0.1 nA and for depletion is ±1 nA. (b) Normalized integrated SPCM line profiles taken at -2 V applied bias. Trace color corresponds to the color scale of the transfer curve in 'a' to indicate the applied gate bias. Grey dashed lines mark the position of the lithographically defined contacts while black dashed lines mark the metal-semiconductor junction of the intruded contacts. Inset shows the photocurrent line profiles before integration and normalization.

has on μ_{FE}. Up until this point, the series resistance of the contacts has been neglected when calculating μ_{FE}. However, for a large series resistance the measured conductance, or external conductance g_{ex}, can deviate significantly from what is known as the intrinsic

conductance, g_{in}. This is described by the following expression[53]

$$\begin{aligned} g_{ex} &= \frac{g_{in}}{1 + g_{in}R_S + (R_S + R_D)/R_{wire}} \\ g_{in} &= \frac{\mu_{FE}C_{ox}}{L^2}V_{DS} \end{aligned}$$

where R_S and R_D are the series resistances of the source and drain contacts, respectively and R_{wire} is the resistance of the nanowire. Assuming an equal contact resistance of 100 kΩ for the source and drain contacts and a wire resistance of 2 MΩ, μ_{FE} is 107 cm^2/V·s when considering the entire device channel. However, if only 1.5 μm of the channel is active and the remaining 4.5 μm is considered a large series resistance (500 kΩ), μ_{FE} becomes 36 cm^2/V·s. In much of the nanowire device literature, devices are analyzed with the assumption that composition does not vary within the device channel in order to simplify the interpretation. However, this result illustrates the potential error in such an assumption.

7.2.1. Field fluctuations

Another observation of the local photocurrent response in the long-channel p-type silicon nanowire FET was the existence of reproducible field fluctuations in the channel. Given the amount of surface doping, a nonuniform photocurrent profile with increasing magnitude toward the tip was expected. However, as seen in Figure 7.8a, short-range fluctuations in the photocurrent signal were observed as well. The noise level for the measurement was less than 10 pA, so the fluctuations observed in the line profiles are a result of actual changes in the photocurrent response rather than noise. As has been discussed

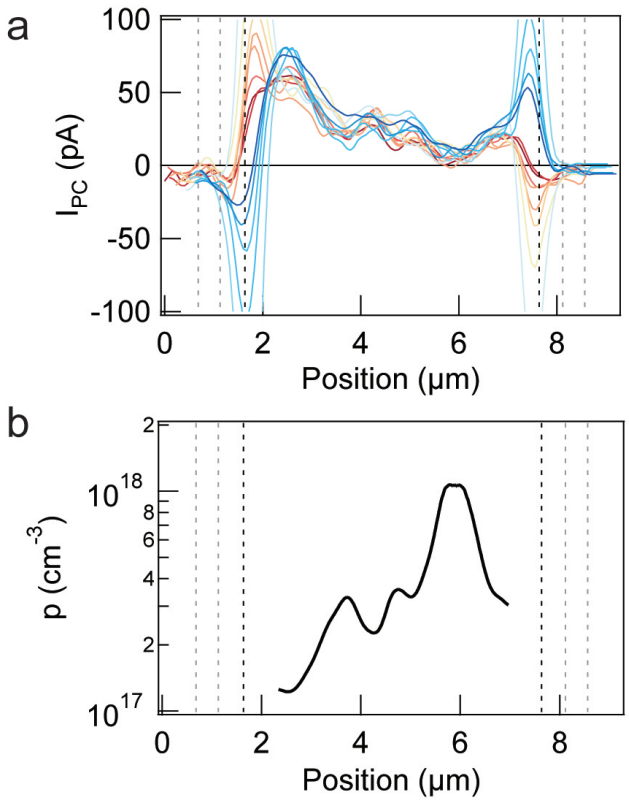

Figure 7.8. SPCM line profiles at low to moderate source-drain bias and extracted effective hold concentration. (a) Bias-normalized SPCM line profiles taken from -0.5 V_{DS} to 0.8 V_{DS} in increments of 0.1 V. Grey dashed lines mark the position of the lithographically defined contacts while black dashed lines mark the metal-semiconductor junction of the intruded contacts. (b) Extracted effective hole concentration within the device channel.

previously (see Chapter 5), the magnitude of the local photocurrent is proportional to $\rho(x)/A(x)$. Other than the diameter taper detailed above, no fluctuations in wire diameter were observed using SEM suggesting that the current fluctuations along the length of the wire are related to changes in the resistivity, ρ. It may be that for boron doping during VLS, fluctuations in the dopant density arise either in the core doping or the surface layer. Applying the same analysis procedure that was used to extract effective electron

concentrations in Chapter 5, the effective hole concentration was extracted to visualize the doping fluctuations. Unfortunately, because of the intruded contacts, an accurate determination of the contact resistance was not possible. Instead it was assumed that the potential drop was equal to the applied bias. As shown in Chapter 5, the majority carrier concentration, in this case holes, is given by

$$\mathrm{p(x)} = \frac{\mathrm{I_{DC}}}{\mathrm{E(x)}} \frac{1}{\mathrm{e}\mu_{\mathrm{p}}\mathrm{A}}. \tag{7.1}$$

The local field,$E(x)$, is proportional to the potential gradient. Therefore, overestimating the potential drop in the channel will overestimate the electric field thereby reducing the calculated effective carrier concentration. Despite the underestimation in carrier concentration, doping level fluctuations can still be analyzed.

As can be seen in Figure 7.8b, there is an increasing hole concentration toward the base of the nanowire, but there are also very large fluctuations. The sampled volume of the semiconductor in SPCM is given by $\pi r^2 w$ where r is the nanowire radius and w is the laser spot size. For this device, the sampled volume is ~3.5×10^{-16} cm^3. At a doping level of 3×10^{17} cm^{-3}, there would be approximately 100 boron atoms in the sampled volume. Considering Poisson statistics, natural fluctuations in a system with randomly distributed dopants will be $\sqrt{\lambda}$ where λ is the number of dopant atoms. In this case Poisson noise can account for fluctuations of up to 10 atoms or 2.8×10^{16} cm^{-3}. It is concluded that the observed field fluctuations cannot be solely attributed to dopant fluctuations arising from Poisson statistics. Instead it may be due to non-uniform dopant incorporation at the surface. Local variations in minority carrier lifetime could also cause changes in the photocurrent.

7.3. Summary

In conclusion, the influence of surface doping on the performance and operation of boron-doped silicon nanowire p-FETs has been studied. It was shown that the subthreshold slope and threshold voltage change monotonically toward the nanowire tip. Devices fabricated in areas of high surface doping show high threshold voltage and degraded subthreshold characteristics due to screening of the electric field from the gate electrode. Furthermore, SPCM was used to qualitatively investigate variations in contact resistance along the length of a boron-doped silicon nanowire. It was found that in regions of heavy surface doping contacts at either end of the device were roughly symmetric. However, for devices near the tip of the nanowire, asymmetry in the contacts was detected by SPCM and under low applied bias the potential drop occurs primarily at the contacts due to high contact resistance.

The effects of surface doping on long-channel devices were also investigated using SPCM. Current-voltage characterization of a long-channel device showed comparable device performance and field-effect mobility to the short-channel devices. However, efficient depletion of the device channel was observed for only the tip-end of the wire causing a shift of the potential drop to just this side of the device. This effectively reduces the active device channel length. Using this effective channel length there was a factor of 3 reduction in the field-effect mobility indicating the importance of understanding device function and material uniformity in the analysis of nanoscale devices. Finally, long-channel devices exhibited fluctuations in the local photocurrent response that was converted to an effective carrier concentration. However, it is still not known if the fluctuations in carrier concentration occur at the surface or in the bulk of the nanowire.

CHAPTER 8

Characterization of n-Si nanowire Schottky diodes

In Chapter 5, it was shown that the photocurrent response within the channel of a two-terminal nanowire device was proportional to the electric field and thus varied linearly with the applied bias. This enabled a quantitative interpretation of the results based on the known potential drop within the device channel. However, in the case of the surface-etched n-FET presented in Chapter 6, only qualitative potential profiles were presented in the absence of a quantitative model of the large photocurrent signals at the n^+-n junctions. The signal observed at these junctions was as much as two orders of magnitude greater than the peak signal observed in unetched devices. Similarly, the contact regions of the unetched devices were not treated in the SPCM analysis because of the signal associated with internal fields at the metal-semiconductor junctions[66]. Given a more complete model for the local photocurrent response, the signal at abrupt junctions may be used to provide quantitative analysis of potential gradients and material properties. For example, the response at the contacts arises due to the Schottky barrier that exists at the metal-semiconductor junctions. The electrostatics of such junctions are well described by existing models, and, as will be discussed below, the internal field is strongly dependent on the doping concentration. Therefore, if a quantitative value for the electric field could be established by SPCM, one could calculate the effective dopant concentration. This is also true for the etched n^+-n junctions; the internal field depends on the Fermi-level

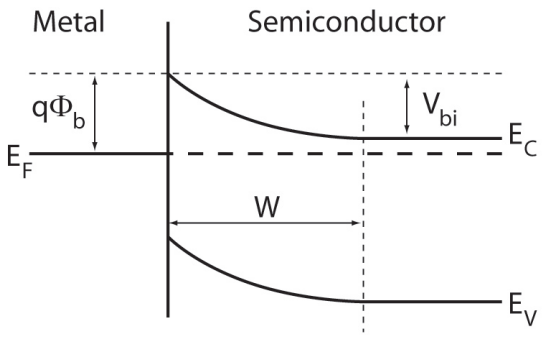

Figure 8.1. Band structure diagram of a Schottky barrier to an n-type semiconductor.

difference between the etched and unetched regions which is directly related to the carrier concentration.

In order to advance the understanding of the local photocurrent response at an abrupt junction, it is necessary to model the electrical characteristics of a well-defined junction with known parameters. In Chapter 4, n-type silicon nanowire Schottky diodes were used to study minority carrier transport. In this chapter, the current-voltage characteristics of these diodes are examined in detail and the magnitudes of internal electric fields are estimated. This result may serve as a basis for additional modeling of the photocurrent response at abrupt junctions in nanowire devices.

Figure 8.1 shows a simplified diagram of the band structure of a Schottky barrier to an n-type semiconductor. On the diagram, three main features of the Schottky barrier are indicated, the barrier height, Φ_b, the built-in potential, V_{bi}, and the depletion width, W. In an ideal Schottky barrier, Φ_b is simply given by the difference between the metal

work function and the electron affinity of the semiconductor. V_{bi} is then given by

$$\mathrm{V_{bi}} = \Phi_\mathrm{b} - \frac{\mathrm{E_F} - \mathrm{E_c}}{\mathrm{q}}, \tag{8.1}$$

where E_c is the conduction band energy, E_F is the Fermi energy of the semiconductor, and q is the electron charge. Using the full depletion approximation, W is given by

$$\mathrm{W} = \sqrt{\frac{2\epsilon_0\epsilon_\mathrm{r}(\mathrm{V_{bi}} - \mathrm{V_a})}{\mathrm{qN_d}}}, \tag{8.2}$$

where N_d is the donor density, ϵ_0 is the permittivity of free space, ϵ_r is the semiconductor dielectric constant, and V_a is the applied bias across the junction. Finally, the maximum electric field occurs at the junction interface and is given by

$$\mathrm{E_{max}} = -\frac{\mathrm{qN_dW}}{\epsilon_0\epsilon_\mathrm{r}}. \tag{8.3}$$

Therefore the maximum field is sensitive to both the Schottky barrier height and the semiconductor doping level. The plots in Figure 8.2 show the scaling of the maximum electric field with electron concentration and barrier height for values based on an ideal Au-Si Schottky diode. The ideal barrier height for a Au-Si junction is ˜0.8 eV, however experimentally this value is reduced by defects and impurities at the Au-Si interface[87,88].

8.1. Fabrication and I-V characterization

In this study, two types of n-type silicon nanowire Schottky diode were investigated. The first is composed of a heavily doped silicon nanowire channel with one Au contact (Schottky) and one Ni contact (Ohmic), identical to the devices used in Chapter 4. The

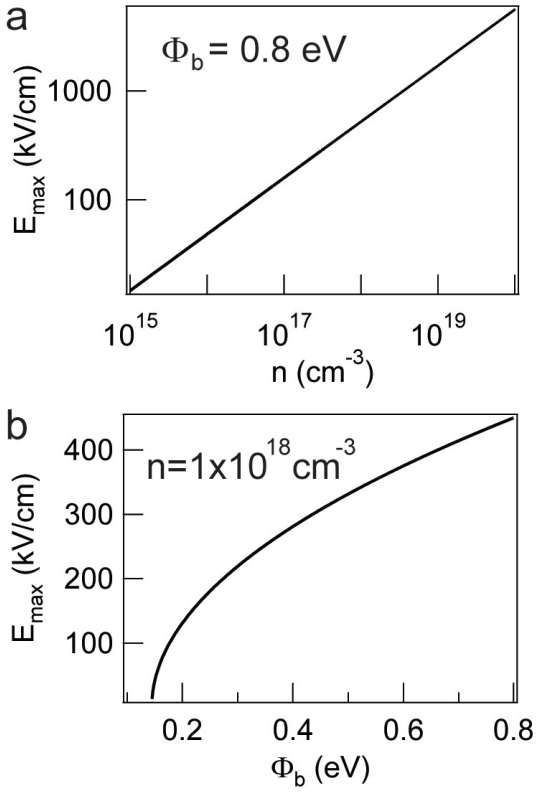

Figure 8.2. Maximum electric field at the Au-Si interface for and ideal Schottky barrier. (a) E_{max} versus electron concentration for the ideal Au-Si barrier height of 0.8 eV. (b) E_{max} versus Schottky barrier height at n=1×10^{18} cm^{-3}.

second type of diode was made using two Ni contacts on a silicon nanowire with varying doping along the length. Based on known nanowire growth rates, wires were synthesized to have three segments of approximately equal length with the base and tip being heavily doped with phosphorous and the middle segment being undoped. Resulting wires were 30-36 μm in length. The doping profile within the wire was confirmed by making multiple devices along a single nanowire and measuring current-voltage characteristics (see Figure 8.3). Devices at either end of the wire show symmetric device current with applied bias while those with one contact near the middle of the wire showed rectifying device behavior.

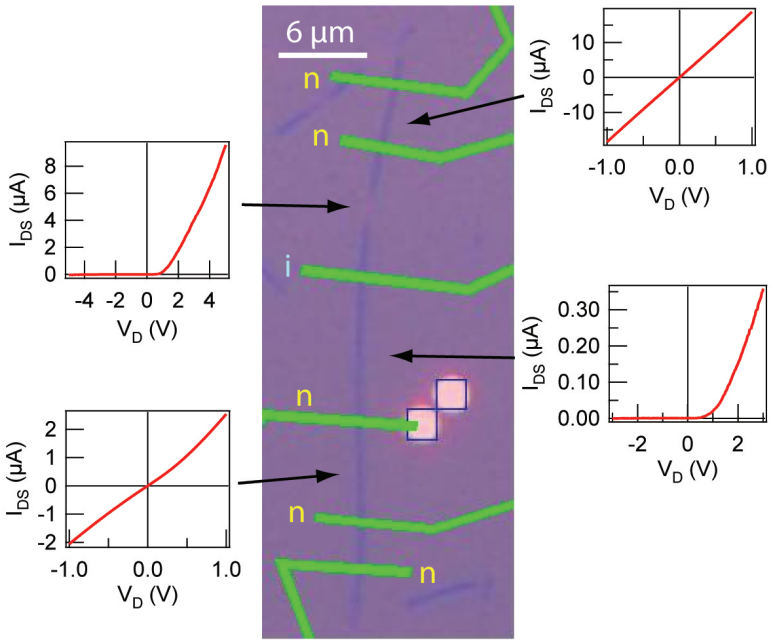

Figure 8.3. Schottky diodes fabricated from modulation-doped silicon nanowires. Devices fabricated at either end of the nanowire show symmetric I-V behavior while those with a contact on the middle segment show rectifying behavior.

In this case the high doping level at the ends of the wire caused a narrowing of the Schottky barrier leading to increased tunneling current and a reduced contact resistance. However, in the middle of the channel the carrier concentration is lower, so the contact resistance is significantly higher. Therefore, having one contact on each segment results in a Schottky diode. It is important to note that growth conditions were comparable to those used for the wires in Chapter 5 for which a surface doping gradient was identified. Undoped silicon nanowires grown by VLS typically show p-type character, however the wires for this study show n-type transport characteristics even in the undoped segments. Therefore, it can be concluded that surface doping is present in these wires. While carrier concentrations

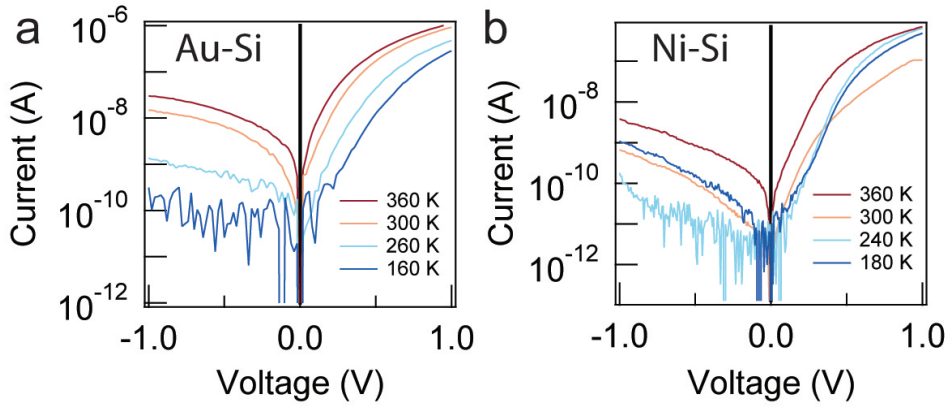

Figure 8.4. Current versus applied voltage at various temperatures for Au-Si, (a), and Ni-Si, (b), Schottky diodes.

are significantly reduced in the middle of the wires compared to the intentionally doped segments, carrier concentrations in these regions may still be quite high.

The characteristics of the Schottky barriers can be determined by analyzing the current-voltage behavior. In an ideal Schottky diode with current dominated by thermionic emission, the forward-bias diode current increases exponentially with applied bias at a rate related to the barrier height. However, in the diodes used for this study, it was expected that there would be increased influence from tunneling because of the high doping concentrations. Current-voltage data was taken at different temperatures for the two diode types, as shown in Figure 8.4. At high forward bias (> 1 V), the series resistance of the nanowire dominated and was fairly similar for these two devices (˜350 kΩ). However, at low bias the characteristics were clearly different for the two types of diode. The Ni-Si diode showed an exponential region under low forward bias that extended to higher bias with decreasing temperature. The Au-Si diode showed no exponential region in the current-voltage data. It is likely that the reduced carrier concentration of the Ni-Si diode

lead to an increased depletion width that reduced the tunneling current. Therefore the expected exponential device current was observed at low bias. However, in the Au-Si case, the semiconductor was heavily doped even in the Schottky barrier region, so the tunneling current was much more significant for this device. This interpretation was further supported by the reduced reverse bias current in the Ni-Si diode.

Using the thermionic-emission diffusion model for planar Schottky diodes, the device current can be described by the following expression[89]:

$$\text{I} = I_0\, exp\left(q\left(V_a - IR\right)/nkT\right)\left[1 - exp\left(-q\left(V_a - IR\right)/kT\right)\right], \tag{8.4}$$

$$\text{I}_0 = AA^{**}T^2 exp(-q\Phi_b/kT). \tag{8.5}$$

Here, I_0 is the saturation current, R is the device series resistance, n is the ideality factor, A is the metal-semiconductor junction area, and A^{**} is the effective Richardson constant (112 A $\text{cm}^{-2}\text{K}^{-2}$ for n-type silicon[37]). For an ideal junction that fits the thermionic-emission diffusion model perfectly, n should be unity while increased values typically are attributed to contributions from tunneling current or interfacial defects. The series resistance for the devices under study was determined from the slope of the current versus voltage plot at high forward bias where the series resistance dominates. The data was then plotted as $ln\{I/\left[1 - exp(-q(V_a - IR)/kT\right]\}$ versus $(V_a - IR)$ and linearly fit in the low bias region where the influence of the series resistance is minimized[88]. From this plot, I_0 and q/nkT can be determined from the y-intercept and slope, respectively. The effective barrier height can be determined from the saturation current if the contact area is known. For this analysis the contact area is estimated to be πrw where r is the wire radius and w is the contact width. This assumes that the entire contact area is involved in

Type	Device	T (K)	n	Φ_b
Au-Si	# 1	160	2.7	0.27
		300	1.7	0.43
		360	1.5	0.49
	# 2	160	2.7	0.27
		300	1.7	0.43
		360	1.5	0.49
Ni-Si	# 1	180	4.0	0.33
		300	2.7	0.51
		360	2.0	0.57
	# 2	180	3.7	0.31
		300	1.9	0.53
		360	1.7	0.57

Table 8.1. Extracted ideality factor and Schottky barrier height from current-voltage analysis of Au-Si and Ni-Si nanowire Schottky diodes.

the diode current, however this is likely not the case. Because of the very small dimensions of the junction, inhomogeneities at the interface could reduce the effective contact area. Furthermore, the typical interpretation of Schottky barriers assumes a planar geometry in which the applied bias results in a field perpendicular to the interface. In this device geometry, the applied field is approximately parallel to the interface which could cause significant current crowding at one side of the contact reducing the effective contact area. There is currently no standard model for the treatment of such a geometry, so a uniform current density across the junction is assumed. The results of this analysis are presented in Table 8.1.

Two devices of each diode type were analyzed and good agreement in the barrier characteristics for each system was observed. The extracted Au-Si barrier height was lower than the Ni-Si barrier by approximately 100 meV at room temperature. Based on the metal work functions of Au and Ni, it is expected that the Ni-Si Schottky barrier will be 0.6 eV compared to 0.8 eV for Au-Si. However, it is likely that the increased carrier concentration in the Au-Si diodes resulted in a reduced effective barrier height because of increased tunneling. This is consistent with the observations made regarding the current-voltage data in Figure 8.4. In both cases the observed barrier heights were significantly lower than the ideal values and decrease with decreasing temperature. The temperature dependence can be explained by considering the influence of tunneling current. At reduced temperatures there will be a decrease in the thermionic emission current over the barrier while the tunneling current will remain largely unchanged. Thus, at reduced temperatures the relative contribution from tunneling current increases causing a larger deviation from ideality. This was also reflected by increased ideality factors at lower temperatures. Woodruff et al.[72] recently reported on the analysis of similarly prepared Ni-Si Schottky diodes using n-type silicon nanowires. They found a room temperature barrier height of 0.49 eV that decreased to 0.34 eV at 200 K for silicon wires with a resistivity of 0.1 Ωcm. Furthermore it was determined that in more highly doped nanowires, the effective barrier height was reduced. These observations are in good agreement with those reported here.

8.2. SPCM determination of V_{bi}

From Equations 8.2 and 8.3, it can be seen that for $V_a = V_{bi}$ the electric field at the metal-semiconductor junction will be zero. This is also known as the flat-band condition.

In the previous chapters, SPCM has been established as a technique that is highly sensitive to local electric fields in nanowire devices. Therefore, SPCM can be used to probe the electric field at the junction to determine the bias required to establish the flat-band condition. For the Au-Si and Ni-Si junctions presented in this study, the SPCM analysis gives V_{bi} values that are approximately 100 meV lower than the extracted barrier heights from Table 8.1. Using the extracted barrier height and measured V_{bi}, effective electron concentration and the maximum internal electric field can be calculated.

SPCM measurements of the nanowire Schottky diodes showed strong signal localized to the near-contact region of the Schottky contacts. The sign of the observed photocurrent was consistent with the expected band bending for an n-type Schottky barrier. Under reverse bias and moderate forward bias the signal remained localized near the Schottky contact. SPCM measurements were conducted at small forward bias steps to identify the flat-band condition. Integrated line profiles of the data are shown in Figure 8.5. This representation of the data is useful for identifying the flat-band condition as the shape of the profiles should be representative of the band bending in the semiconductor at the metal-semiconductor junction (see discussion of n^+-n junctions in Chapter 6). For the Au-Si Schottky diode, a flat-band voltage of ~0.35 V is determined from SPCM. Using Boltzmann statistics to expand on Equation 8.1 for the built-in voltage gives the expression:

$$\mathrm{V_{bi}} = \Phi_\mathrm{b} - \frac{(\mathrm{E_{Fi}} - \mathrm{kT}\ \ln(\mathrm{n}/\mathrm{n_i})) - \chi}{\mathrm{q}}. \tag{8.6}$$

In this equation, E_{Fi} is the intrinsic Fermi energy for silicon, n_i is the intrinsic electron concentration, and χ is the electron affinity. Using the extracted barrier height from

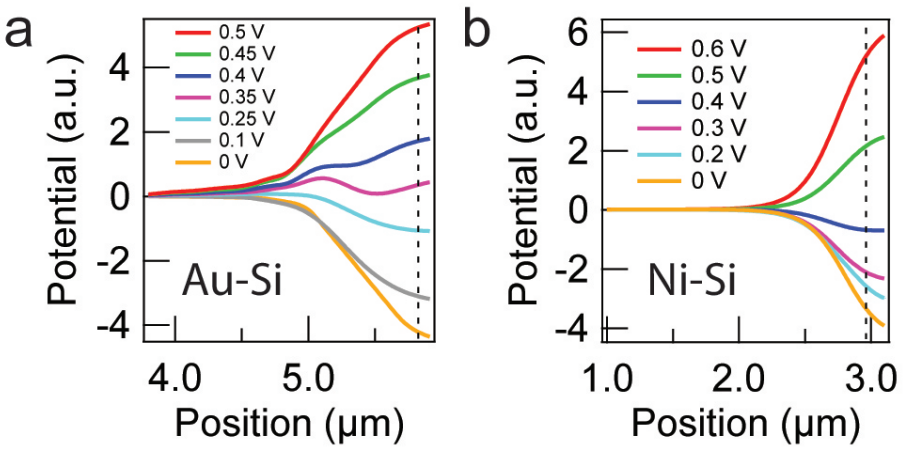

Figure 8.5. SPCM determination of V_{bi} in nanowire Schottky diodes. (a) Pseudo potential profiles of a Au-Si nanowire Schottky diode at the indicated forward biases ($V_{bi} \approx 0.35\ V$). (b) Pseudo potential profiles of a Ni-Si nanowire Schottky diode at the indicated forward biases ($0.4\ V < V_{bi} < 0.5\ V$).

Table 8.1 ($\Phi_b = 0.43\ eV$) and the measured V_{bi} from SPCM ($V_{bi} = 0.35\ eV$), the carrier concentration, n, in Equation 8.6 is 1.2×10^{18} cm^{-3}. SPCM analysis of the Ni-Si diode suggests a built-in potential of just over 0.4 eV. In this case, using $\Phi_b = 0.53\ eV$ and $V_{bi} = 0.41$ to $0.43\ eV$ gives an electron concentration of 3 to 6×10^{17} cm^{-3}. The Boltzmann approximation is not technically correct for the doping levels of interest in this study, however the error results in an underestimation of the electron concentration by only 15% for the Au-Si diode. This approximation also neglects band gap narrowing which will have an effect on not only V_{bi}, but the Schottky barrier height as well. The expected change in the position of the conduction band in going from 5×10^{17} cm^{-3} to 1.2×10^{18} cm^{-3} electron concentration is only 5×10^{-3} eV[37], so this does not introduce significant error in the calculation. Still, these considerations must be kept in mind as the error will get larger with increasing carrier concentation.

The estimated carrier concentrations in this calculation are lower than those obtained from SPCM measurements in Chapter 5 by a factor of ten. The carrier concentration extracted from diode device performance is related only to the carrier concentration at the metal-semiconductor interface which could be reduced due to HF-etching the surface before contact deposition. Furthermore, from Equation 8.6 it can be seen that n will depend strongly on the difference of V_{bi} and Φ_b. Considering only a $\pm$ 50 mV error in both V_{bi} and Φ_b accounts for variation in the estimated electron concentration over four orders of magnitude.

As mentioned previously, knowledge of the internal fields at abrupt junctions in nanowire devices will facilitate quantitative correlation of the local photocurrent response from SPCM with material properties. Using the extracted Schottky barrier parameters described above, it is possible to calculate the maximum electric field at the metal-semiconductor junctions in these devices. For the Au-Si junction, E_{max} is approximately 3.5×10^5 V/cm while for the Ni-Si junction the field is ˜2 to 3×10^5 V/cm. In both cases the field is two to three orders of magnitude higher than the measured field in the channel of ohmic silicon nanowire devices presented in Chapter 5. Therefore, one would expect an increase of two orders of magnitude in the local photocurrent at this type of junction assuming that the field remains high throughout the generation region. However, the expected depletion width based on these Schottky barrier properties is very short (W=30-160 nm) even for reverse biases as high as 10 V (see Figure 8.6). In Chapter 5, the local photocurrent of an unetched silicon nanowire device was shown to vary between 100 and 200 pA in the device channel while photocurrent peaks of 100 to 200 nA were measured at the n^+-n junctions of the etched devices in Chapter 6 using ˜1/4 the

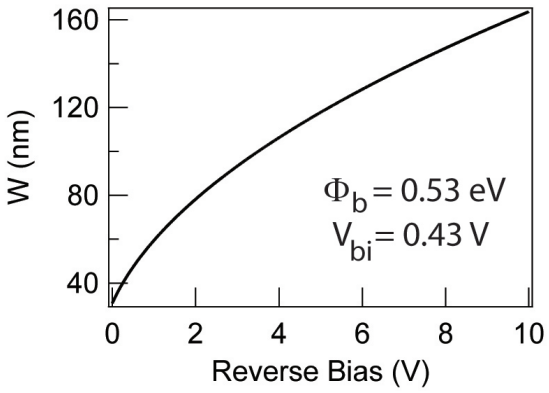

Figure 8.6. Depletion width of a Ni-Si Schottky barrier versus applied reverse bias. Parameters for the calculation were taken from the estimates in the main text.

excitation intensity. Considering that most of the excess carrier generation occurs at a distance greater than W away from the junction, a peak current increase of over three orders of magnitude cannot be explained in terms of a constant proportionality between the field and the photocurrent. A quantitative description of the magnitude of the local photocurrent will require additional modeling of the photocurrent response allowing for large variation of the electric field within the generation region.

8.3. SPCM under forward bias - locating the n-i junction

For the Ni-Si Schottky diode SPCM studies, silicon nanowires containing axial n-i homojunctions were used. Under large forward bias, the photocurrent signal extends into the device channel as the resistances of both the Schottky barrier and the n^+-n junctions are reduced. The undoped segment of the device channel becomes the dominant resistance creating an electric field that can be detected using SPCM. Because the field is much larger in the lightly-doped segment of the channel, the location of the n-i junction in these

devices is readily identified. Figure 8.7a shows a schematic of the device geometry used to demonstrate this point. Three contacts were fabricated on a long nanowire composed of three segments, n^+-i-n^+. The two outer electrodes contact the heavily doped segments while the middle electrode contacts the undoped region. For the purpose of this measurement, this structure will be treated as two independent two-terminal devices. The first is defined by the left and middle electrodes. Upon applying a negative bias to the left electrode, the n^+-n junction in the channel and the Schottky barrier at the middle electrode will be under forward-bias. With increasing applied bias, a potential drop occurs in the undoped region of the nanowire creating an electric field. The red data in Figure 8.7b was acquired with -4 V applied bias. Similarly, the second device, defined by the middle and right contacts, was forward biased by applying a negative bias to the right electrode. The blue data in Figure 8.7b was acquired with -4 V applied bias on the right electrode. The image was generated by overlaying the results of two separate scans on top of an optical image of the device. The channel lengths are approximately equal; however the device on the left has a mostly undoped channel while the other is mostly doped. For the device on the right, only a small portion (~1.5 μm) of the device channel showed a photocurrent response while the device on the left showed a response over approximately 8.5 μm of the channel. The SPCM results can be used to quantitatively determine the extent of the undoped segment of the wire. In this case, the undoped region is 10.8 μm which is close to the intended length of 12 μm from the nanowire synthesis. Furthermore, Figure 8.7d shows the forward bias current for the two Schottky diodes versus the applied bias. The Schottky barrier analysis from the previous section suggests that the resistance of

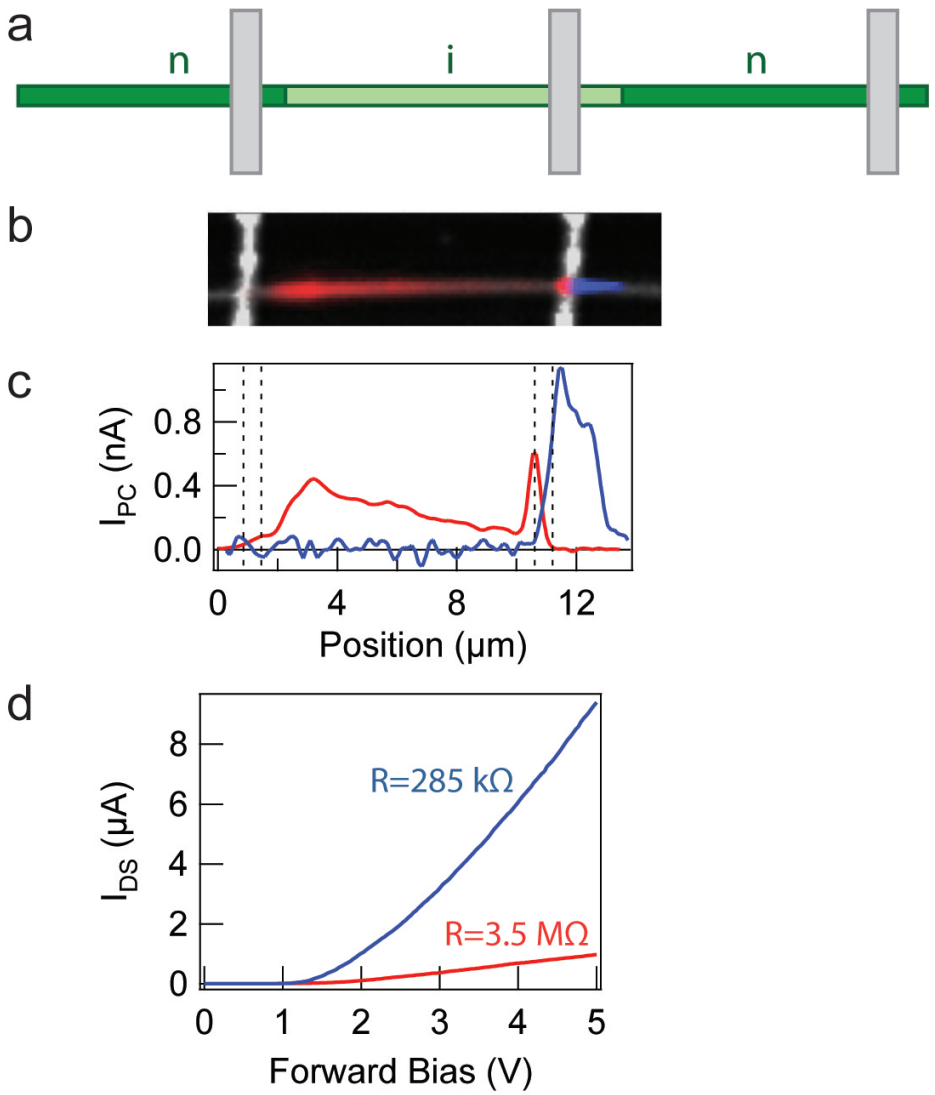

Figure 8.7. SPCM determination of n-i junctions in modulation-doped nanowire Schottky diodes. (a) Schematic of a three-terminal device fabricated on an n^+-i-n^+ silicon nanowire. (b) Optical image (grayscale) with overlayed SPCM data (red and blue). Local photocurrent maps were acquired using -4 V applied bias. (c) Line profiles of the data in 'b'. Total extent of the lightly doped region is 10.5 μm. (d) Forward bias current versus applied voltage for the devices pictured in 'b'. Curves are colored to match the SPCM data and line profiles. The two terminal resistance measured at high forward bias is indicated on the plot for each curve.

the metal-semiconductor junction for the two diodes is comparable. Therefore, the ~12× greater resistance of the left device is due to the increased length of the undoped region.

8.4. Summary

In this chapter, two types of nanowire Schottky diodes were characterized by current-voltage analysis and SPCM. Using typical planar device models it was shown that effective device parameters can be extracted from the two-terminal current versus voltage data. Variable temperature data indicates an increase in the relative contribution from tunneling at reduced temperatures, and an overall reduction in the barrier height compared to expected values was observed. The extracted barrier height for the Au-Si diode was 0.43 eV compared to the ideal value of 0.8 eV, and for the Ni-Si diode the extracted barrier height was 0.53 eV whereas the ideal barrier height is 0.6 eV. SPCM was used to probe the local electric field at the metal-semiconductor junction as a function of the applied bias. It was shown that going from an unbiased device to forward biased results in a sign change of the signal at the contact. By using small bias increments it was possible to identify the flat-band voltage for each device which is equal to the diode built-in voltage. The results are consistent with the extracted barrier heights. Using the barrier height and built-in voltage, estimated effective electron concentrations of 1.2×10^{18} cm^{-3} and 3 to 6×10^{17} cm^{-3} were calculated for the heavily doped and unintentionally doped nanowires, respectively.

From these results the maximum electric field at the junction was estimated to be as high as 3.5×10^{5} V/cm. This is over two orders of magnitude higher than the highest electric field measured in the channel of the devices in Chapter 5. However, the expected

depletion width based on these Schottky barrier properties is very short. It is unclear what the effect of a high field over short-range has on the local photocurrent response. Additional modeling is required to quantify the expected contribution. Furthermore, it was shown that SPCM could be used to identify the location of axial homojunctions in modulation doped silicon nanowires. Under high forward bias, a potential drop occurs in the resistive portion of the nanowire channel enabling localization of the n-i junction.

CHAPTER 9

Summary and future directions

Semiconductor nanowires show great potential as components for bottom-up nanoscale electronics, however there is still a long way to go before nanowire-based devices will become commercially viable. Aside from the obvious challenges in large-scale device integration, the nanowire materials themselves must be optimized in order to improve performance. Currently, there are very few methods for reliable electronic property measurements in nanoscaled materials such as semiconductor nanowires.

In this work, the application of SPCM and EBIC for the quantitative determination of electronic properties in silicon nanowire devices was presented. For the first time, it was shown that minority carrier diffusion lengths in phosphorous-doped silicon nanowires are significantly reduced from their bulk values because of nonradiative recombination at the nanowire surface. Thin film processing of silicon surfaces to yield high quality interfaces is routine, however these results reveal a potentially large hurdle for high performance nanowire optoelectronics. Without clearly defined bounding surface planes, passivation of surface states may be a considerable challenge and will likely never approach the surface quality of planar silicon. However, improvements in the surface state density of one to two orders of magnitude should be possible based on values for non-optimal crystal orientations in planar Si-SiO_2 interfaces[61]. Further experiments along these lines using both organic and inorganic passivation schemes are important for the future of nanowire-based electronics.

SPCM analysis of two-terminal ohmic n-type silicon nanowire devices revealed a nonuniform electric field along the channel length suggesting an increased resistivity toward the nanowire tip. Etching of the nanowire surface eliminated the gradient indicating that the origin was a surface doping profile. Surface doping during VLS growth of nanowires could significantly limit the applicability of this technique for the synthesis of complicated structures. However, it is possible that surface doping could be significantly reduced or eliminated entirely using a different reactor design, such as a cold-wall reactor, and optimized growth conditions. It was shown that SPCM has the sensitivity to detect nonuniform doping and is therefore a useful tool in further efforts to solve the surface doping problem. Furthermore, a method for extracting quantitative potential profiles and effective carrier concentrations was presented. This extends the quantitative utility of SPCM analysis which has previously been used primarily as a qualitative tool.

An additional consideration arising from a radial doping profile was brought to light from the surface etching studies. It was shown that n^+-n junctions are formed at the edges of the etched regions. This can have significant effects on device operation as was observed in EBIC measurements of nanowire Schottky diodes where increased current signal was associated with the edge of the electrode undercut region. However, this effect can also be utilized in devices. High-performance nanowire n-FETs were fabricated by surface etching of an n-type silicon nanowire. In the subthreshold regime, the dominant resistance in the device becomes the n^+-n junctions at the edges of the etched region while in the on-state modulation of the carrier concentration in the etched channel determines the device transfer characteristics.

The effect of nanowire nonuniformity on FET performance was investigated using tapered boron-doped silicon nanowires. The transistor threshold voltages and subthreshold slopes were shown to change monotonically along the length of the nanowire with improved transistor characteristics at the tip. However, the field-effect mobilities extracted from the device transfer curves do not show the same improvement. Presumably this is because of large series resistances introduced at the contacts. The relative contribution from contact restistance was found to increase toward the nanowire tip where the carrier concentration is reduced in the absence of significant surface doping. These results highlight the importance of developing methods to create highly uniform nanowires in order to facilitate repeatable large-scale integration of nanowire devices with reliable characteristics. Additionally, it was emphasized that neglecting compositional and geometrical nonuniformities in the analysis of nanowire devices can lead to significant deviations in calculated material parameters.

Finally a combination of current-voltage analysis and SPCM was used to investigate silicon nanowire Schottky diodes. Schottky barrier properties obtained by the two methods show good agreement and were used to estimate the internal electric field at the metal-semiconductor junction as well as the effective carrier concentration of the semiconductor. This is the first reported application of SPCM for the determination of the built-in voltage in a nanowire Schottky barrier. Using SPCM in conjunction with typical device performance analysis resulted in a more complete characterization of the metal-semiconductor junction in Ni-Si and Au-Si nanowire Schottky diodes. However, future efforts should be focused on developing models to accurately describe the electrostatics of

nanowire Schottky diodes whose geometry deviates significantly from the typical planar junction.

In each case described above, not only was knowledge gained regarding fundamental materials characterization of silicon nanowires, but new and expanded analysis procedures were developed that may be applied to a variety of other materials systems and complicated device structures. To further improve these techniques, accurate quantitative models for the induced current signals must be developed. The present analysis requires that excess carriers are confined to the excitation region in a relatively uniform electric field. This is sufficient to describe long-channel devices fabricated using uniformly doped nanowires. However, for short-channel devices or those consisting of more complicated structures, it becomes necessary to consider the effects of non-uniform fields over very short range and transport of excess carriers outside of the generation region. With a complete model, quantitative potential profiles could be extracted from SPCM data for devices including arbitrary variation in composition and geometry.

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APPENDIX A

Comparison of SPCM and EBIC results

During the course of this work, SPCM and EBIC were used to study nanowire devices. In Chapter 3 it was mentioned that the techniques are analogous in that they both use locally injected charge carriers as a probe for local electrostatic information. This appendix contains a direct comparison of EBIC and SPCM data on a single nanowire device. The SPCM data was taken on a different confocal microscope than the data in the main document and suffers from significantly lower resolution because of poor focus. Also, the excitation wavelength was 457 nm compared with 532 nm for SPCM measurements in the main text. It will be shown that SPCM and EBIC give similar results for the devices studied.

Figure A.1a shows EBIC and SPCM images of the same n-Si nanowire device with a 0.5 V applied bias. Surprisingly, the induced current from the two techniques is almost of the same magnitude. Considering the considerably smaller excitation region for EBIC, this indicates an increased excess carrier concentration. The line profiles in Figure A.1b both show a nonlinearly decreasing induced current signal within the device channel. This is likely due to surface doping as discussed in Chapter 5. The resolution of the EBIC measurement is clearly superior and is able to resolve smaller features than SPCM. An example of this is shown in Figure A.2. At approximately 4.2 μm in the line profiles there is a very sharp decrease in the induced current from the EBIC data. While there is some evidence of this feature in the SPCM line profile, without the EBIC data this would likely

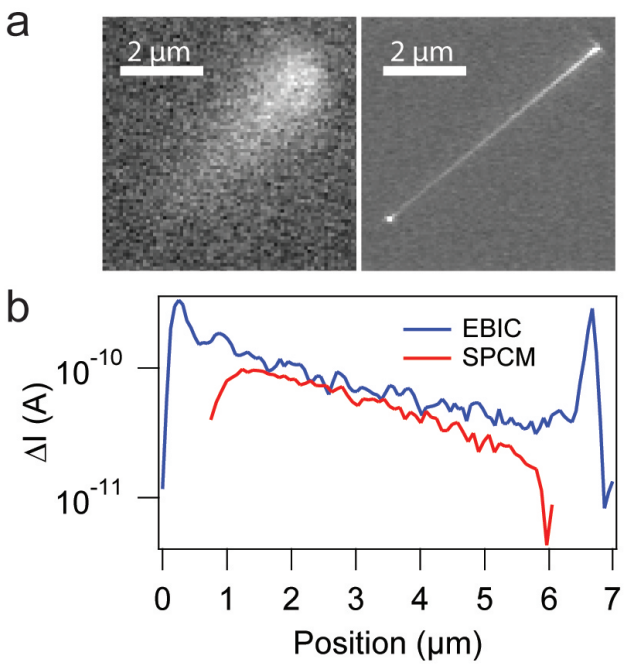

Figure A.1. Comparison of EBIC and SPCM measurement of an n-Si ohmic nanowire device. (a) EBIC and SPCM image of the same nanowire device. Scans were taken at 0.5 V applied bias. (b) Line profiles of the data in 'a' taken along the nanowire axis.

be interpreted simply as noise. The EBIC data also shows large peaks in the signal near the contacts. It is not clear why there are not similar increases in signal in the SPCM data, but it appears to be a result of insufficient resolution. In SPCM, the induced carriers are spread over a large area while for EBIC there is a much more focused excitation of injected carriers. Therefore it is possible that in the near contact region there will be significantly higher charge carrier collection for the EBIC measurement resulting in large signal in these areas. The photocurrent signal in SPCM is averaged over a ~500 nm area so it is expected that the increase in signal near the contacts will be significantly lower and may require improved signal-to-noise to detect.

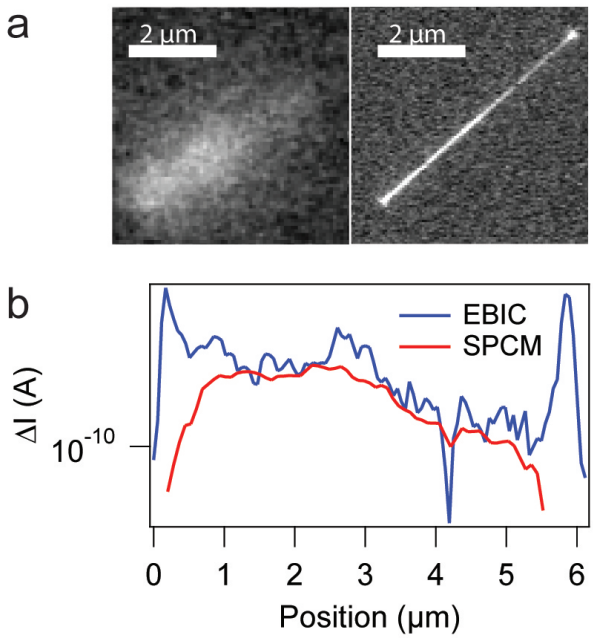

Figure A.2. Comparison of EBIC and SPCM measurement of an n-Si ohmic nanowire device. (a) EBIC and SPCM image of the same nanowire device. Scans were taken at 1 V applied bias. (b) Line profiles of the data in 'a' taken along the nanowire axis.

The high resolution of EBIC makes it an appealing technique for the study of nanostructured materials. However, as was discussed in Chapter 4, there are a number of considerations to make when conducting the measurement. The high energy electron beam could damage the material under study or cause carbon deposition. Also, charging could significantly impact the electrostatics of a device during analysis.

APPENDIX B

SPCM of InAs nanowire devices

In addition to the experiments involving silicon and CdS nanowires, SCPM measurements were conducted on InAs nanowire devices. As with the data presented in Appendix A, this data was taken using a different confocal microscope than the data in the main body of the document. In general, this means the laser focus was poor and the excitation intensity was not known (though the laser power at the source was known). Excitation wavelength was 457 nm.

Two-terminal Ohmic InAs nanowires devices were fabricated by the procedure detailed in Chapter 3. The nanowires used for these measurements were highly tapered. From the discussion in Chapter 5, it is expected that a tapered structure will lead to an increased photocurrent response at the thinner end of the device channel. Figure B.1 shows SPCM results on a typical InAs nanowire device. A local photocurrent response is observed throughout the device channel with maximum occurring at the thin end. This is consistent with the response of tapered silicon nanowires. While this particular device was not characterized by SEM or AFM, based on typical values from this batch of nanowires the diameter in the device channel likely varies from ~40 nm at the thick end to ~20 nm at the thin end. The reduced diameter leads to a higher local electric field and hence an increased photocurrent. Furthermore, it has been suggested that for InAs of diameters $<$ 20 nm, the wires are fully depleted[90]. In this case the effect of taper may be magnified.

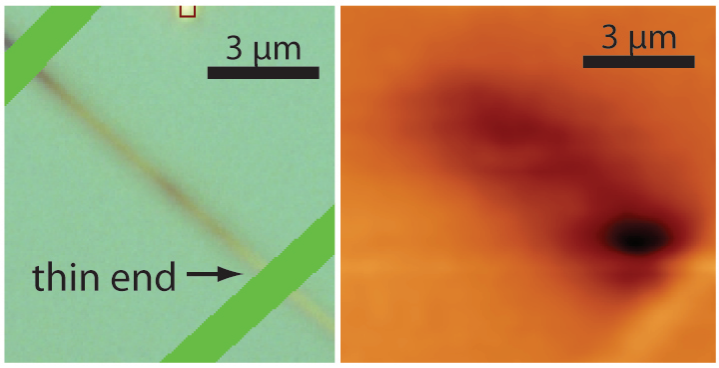

Figure B.1. SPCM measurements of an InAs nanowire device showing the effect of taper. Optical image of the device, (a), and corresponding local photocurrent map, (b). Applied bias was -10 mV. Dark contrast represents a positive photocurrent response. Significantly enhanced signal is observed at the thin end of the nanowire device.

Increasing the excitation laser power lead to a dramatic change in the SPCM response. As shown in Figure B.2, an increase in laser power from 0.1 mW to 0.5 mW reversed the sign of the photocurrent response. Furthermore, it can be seen from the image that a positive photocurrent response exists when the excitation is near the wire, but the signal switches to a negative photocurrent response when the laser is focused directly on the nanowire. This is consistent with an intensity dependence. When the laser is close to the wire but not directly focused onto it, only a fraction of the total laser intensity will be incident on the semiconductor. The current vs voltage data in Figure B.2c was taken as a DC measurement with a continuous excitation. This rules out any possible phase shift that may have caused an apparent sign reversal in the AC measurement. The conductivity of a semiconductor is given by

$$\sigma = e\mu_p p + e\mu_n n. \tag{B.1}$$

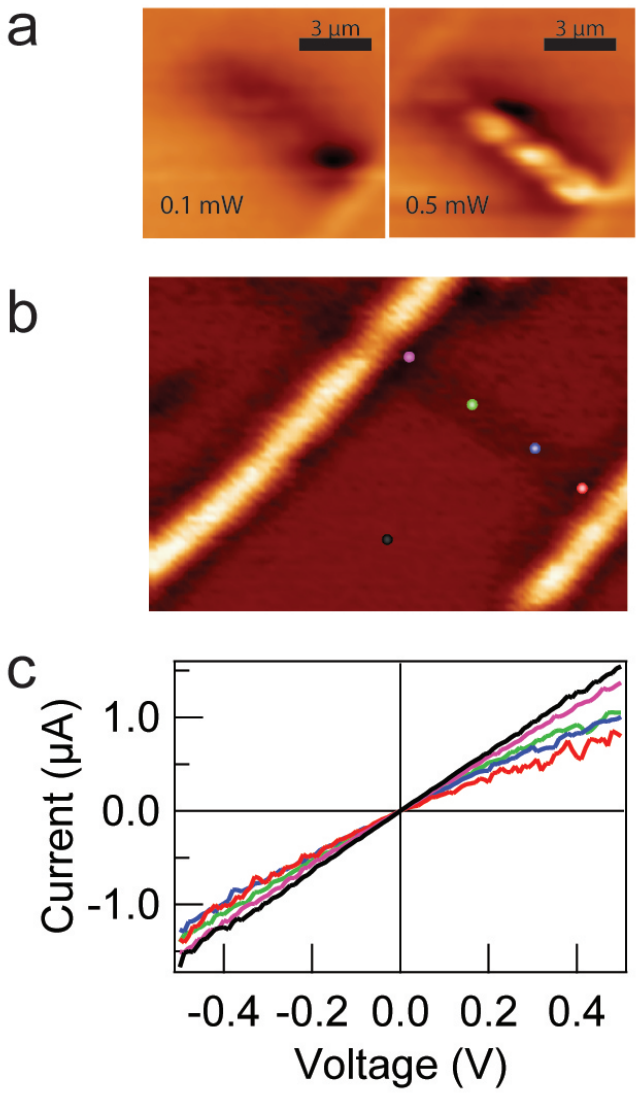

Figure B.2. Negative photoconductivity in InAs nanowire devices. (a) SPCM images of an InAs nanowire device with 10 mV applied bias taken at 0.1 mW (left) and 0.5 mW (right). (b) Reflection image with colored dots marking the location of excitation for the I-V data presented in 'c'. (c) I-V data taken under local illumination. The color of each curve corresponds to the dots in 'b' that indicate the location of the laser spot.

Therefore,

$$\Delta\sigma = e\Delta\mu_p\Delta p + e\Delta\mu_n\Delta n. \tag{B.2}$$

The origin of the negative photoconductivity is not known, but from equation B.2 it is clear that it must be a result of either a reduction in the carrier concentration or the mobility. Because of the high coefficient of absorption for InAs at the excitation wavelength, it is likely that the measurements were conducted under high injection. However, since the excitation power is not known, it is not possible to estimate the excess carrier concentration. The role of heating must also be considered. In InAs, the carrier mobility drops off rapidly with increased temperature[91]. Direct heating of the InAs nanowire most likely does not explain the reduced conductivity as it would be associated with a much larger increase in carrier concentration. However, if the transmitted illumination heats the substrate below the wire, it is possible that there is excessive heating of the wire in the absence of direct absorption. Furthermore, there could be a strong influence of interface states between the nanowire and the device substrate. Further experiments would be necessary to determine the role of this interface on the photoconductivity.

APPENDIX C

Nanowire growth chart

	Growth	Au (nm)	Dopant source	Dopant:Si	T (°C)	P (Torr)	Carrier Gas	Flow Rates (SCCM) carrier/dopant/SiH_4	Time (min)
Chapter 4	EH003A	20	PH_3 (200 ppm in H_2)	500:1	460	40	H_2	30/20/2	20
	EH007C	100	PH_3 (200 ppm in H_2)	500:1	460	40	H_2	30/20/2	12
	EH008A	20	PH_3 (200 ppm in H_2)	1000:1	460	40	H_2	40/10/2	12
	EH035B	50	PH_3 (200 ppm in H_2)	1500:1	460	40	H_2	43.3/6.7/2	12
	EH035C	100	PH_3 (200 ppm in H_2)	1500:1	460	40	H_2	43.3/6.7/2	12
	EH036B	50	PH_3 (200 ppm in H_2)	1500:1	460	40	H_2	43.3/6.7/2	6
	EH036C	100	PH_3 (200 ppm in H_2)	1500:1	460	40	H_2	43.3/6.7/2	6
	EH040B	80	PH_3 (200 ppm in H_2)	1000:1	460	40	H_2	40/10/2	9
	EH040C	100	PH_3 (200 ppm in H_2)	1000:1	460	40	H_2	40/10/2	9
	EH041A	20	PH_3 (200 ppm in H_2)	500:1	460	40	H_2	30/20/2	9
	EH045A	30	PH_3 (200 ppm in H_2)	2000:1	460	40	H_2	45/5/2	9
	EH045B	80	PH_3 (200 ppm in H_2)	2000:1	460	40	H_2	45/5/2	9
	EH086B[1]	50	PH_3 (200 ppm in He)	690:1	460	40	N_2	40/14.5/2	9
	EH086C[1]	80	PH_3 (200 ppm in He)	690:1	460	40	N_2	40/14.5/2	9
Chapters 5 & 6	EH187B	50	PH_3 (200 ppm in He)	500:1	460	40	N_2	30/20/2	15
Chapter 7	EH222	20	B_2H_6 (100 ppm in He)	3000:1	440	40	He	33.3/6.7/4	10
Chapter 8	EH187B	50	PH_3 (200 ppm in He)	500:1	460	40	N_2	30/20/2	15
	JLIV399[2]	50	PH_3 (200 ppm in He)	500:1	450	40	He	30/20/2	12
				undoped	450	40	He	50/0/2	9
				500:1	450	40	He	30/20/2	12

[a]Wires used for oxidation study. Catalyst was etched before oxidizing at 700 °C for 30 min.

[b]Three-stage growth of n-i-n silicon wires. Conditions are given for each growth segment.

Table C.1. Growth conditions for the nanowires used in this work.